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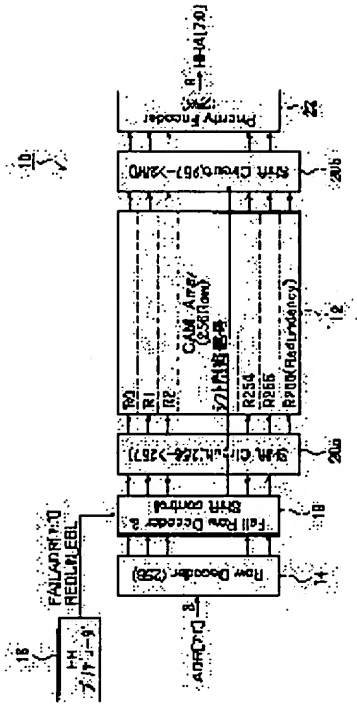
HATA RYUICHI

(54) ASSOCIATIVE MEMORY

(57)Abstract:

PROBLEM TO BE SOLVED: To incorporate a spare CAM word as a redundancy circuit and to improve yield of products without increasing circuit scale and an output delay time.

SOLUTION: This associative memory incorporates a spare CAM word as a redundancy circuit in addition to a plurality of CAM words. Address information of a defective CAM word included in a plurality of CAM words, the memory is controlled so that a defective CAM word is substituted by a spare CAM word conforming to address information of the defective CAM word, an address of the defective CAM word is substituted by an address of the spare CAM word, while an detection coincidence output of the defective CAM word is substituted by an detection coincidence output of the spare CAM word.



LEGAL STATUS

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[Date of final disposal for application]

[Patent number]

[Date of registration]

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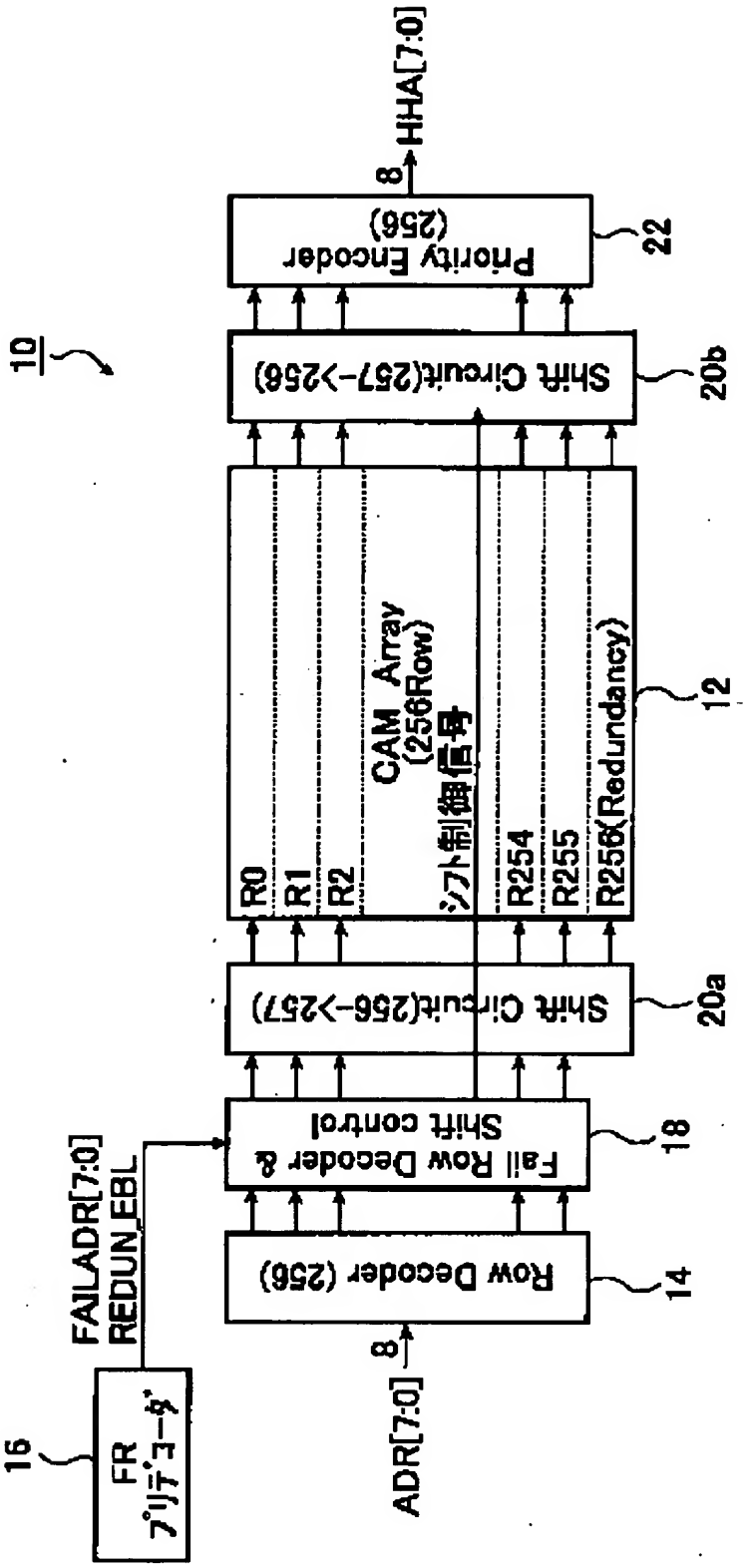
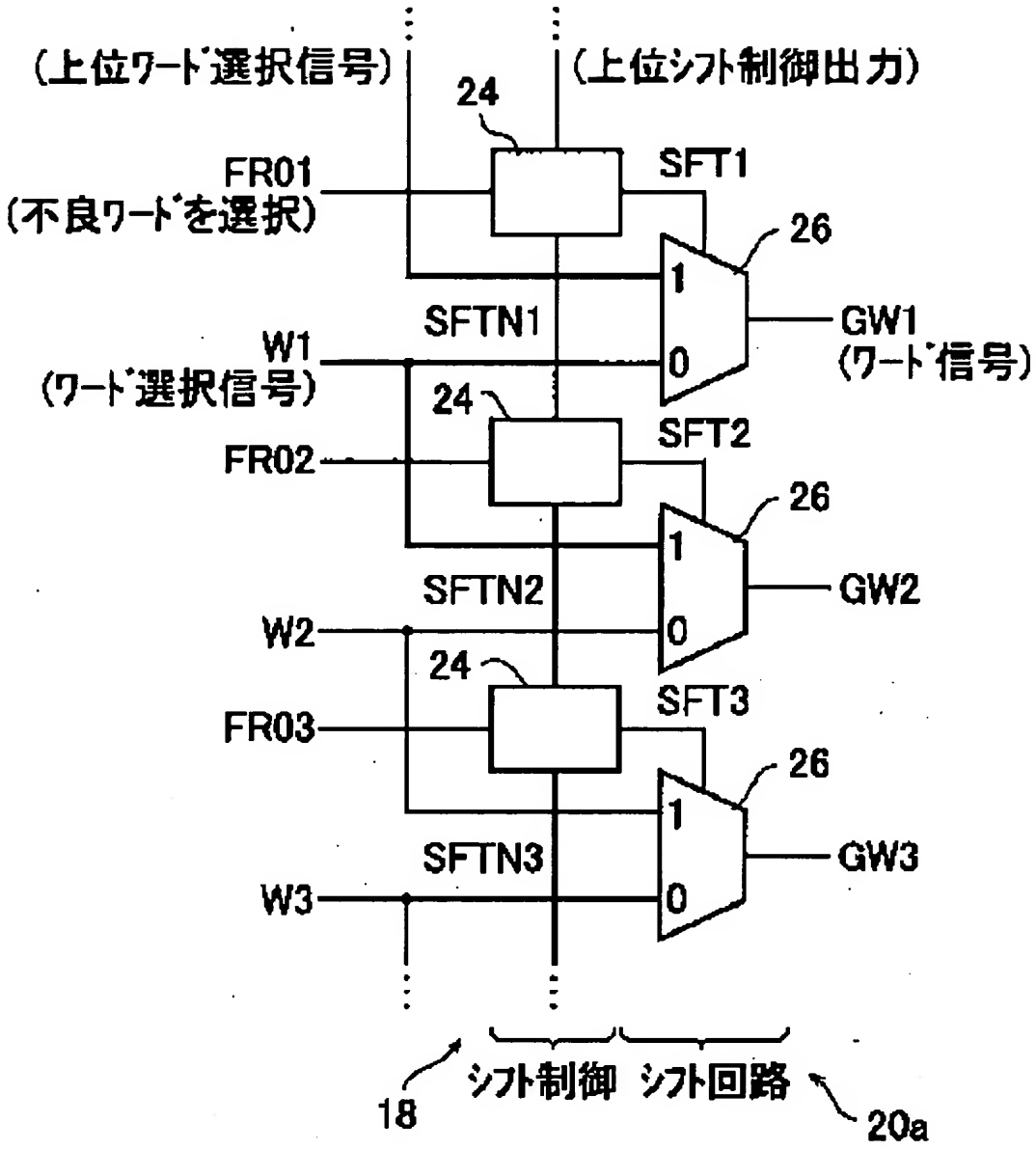
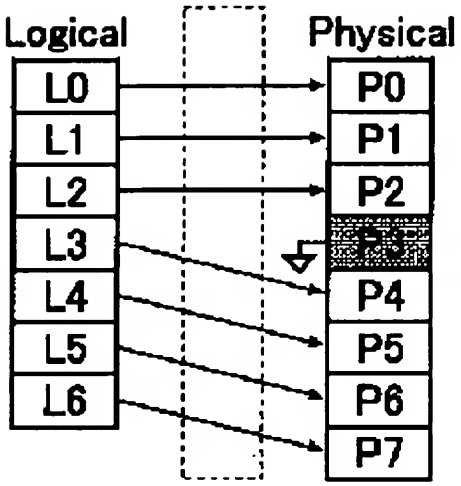
[Date of requesting appeal against examiner's decision of rejection]

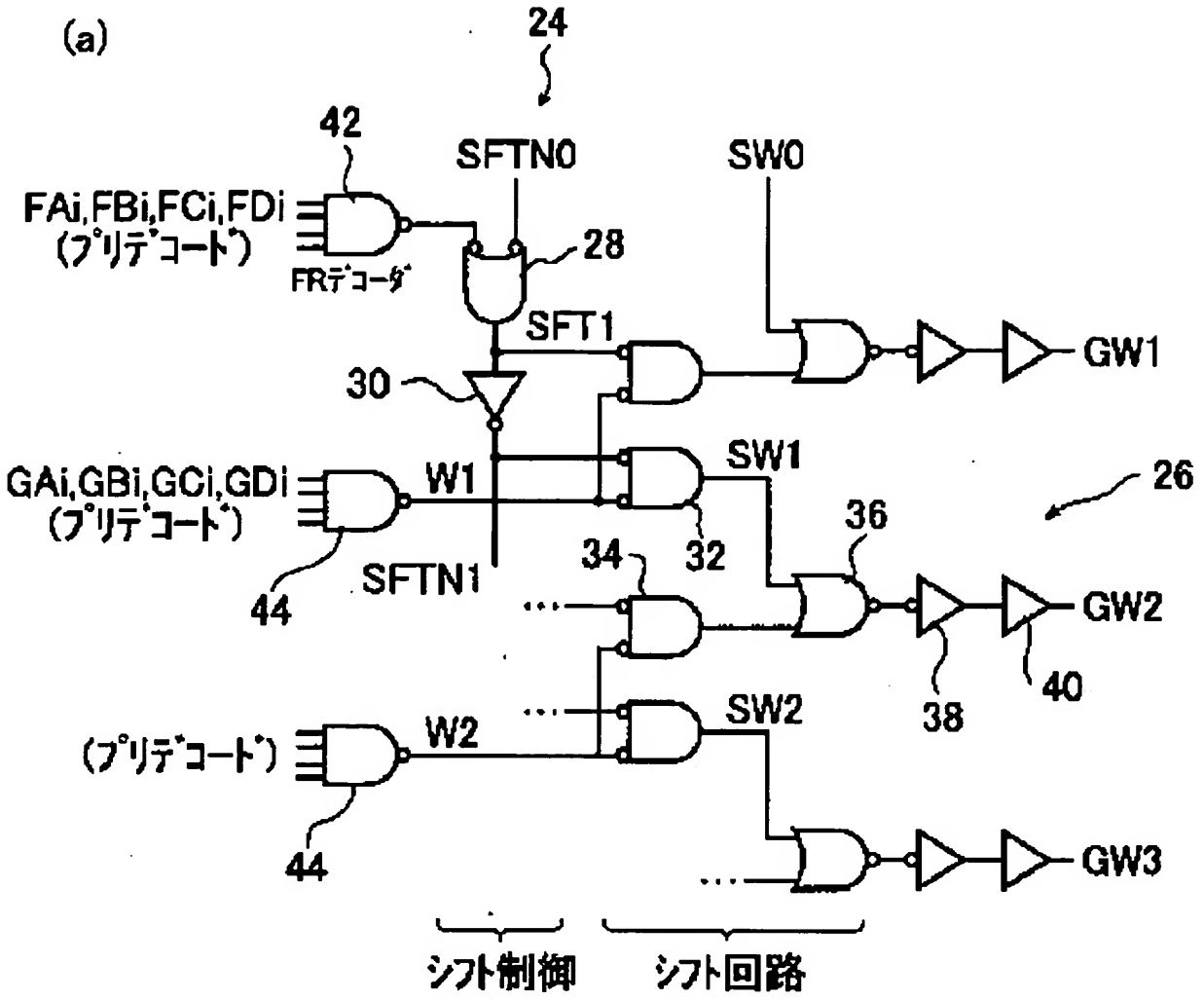
[Date of extinction of right]


10
16
FR
ﾌﾘﾃﾞｺｰﾀﾞ
FAILADR[7:0]
REDUN_EBL
ADR[7:0]
8
14
Row Decoder (256)
18
Fail Row Decoder &
Shift control
20a
Shift Circuit(256->257)
12
CAM Array
(256Row)
ｼﾌﾄ制御信号
R0
R1
R2
R254
R255
R256(Redundancy)
20b
Shift Circuit(257->256)
22
Priority Encoder
(256)
8
HHA[7:0]

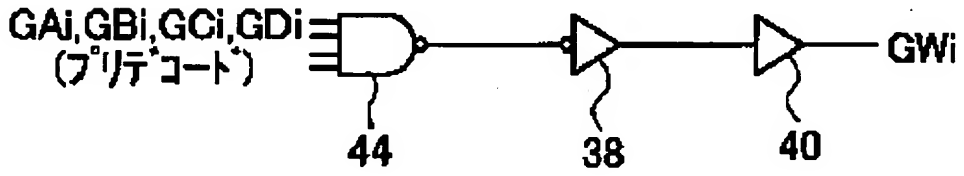

(上位ワード選択信号)
(上位シフト制御出力)
24
FR01
(不良ワードを選択)
SFT1
26
1
SFTN1
GW1
(ワード信号)
W1
(ワード選択信号)
0
24
SFT2
FR02
26
1
SFTN2
GW2
W2
0
24
SFT3
FR03
26
1
SFTN3
GW3
W3
0
18
シフト制御
シフト回路
20a

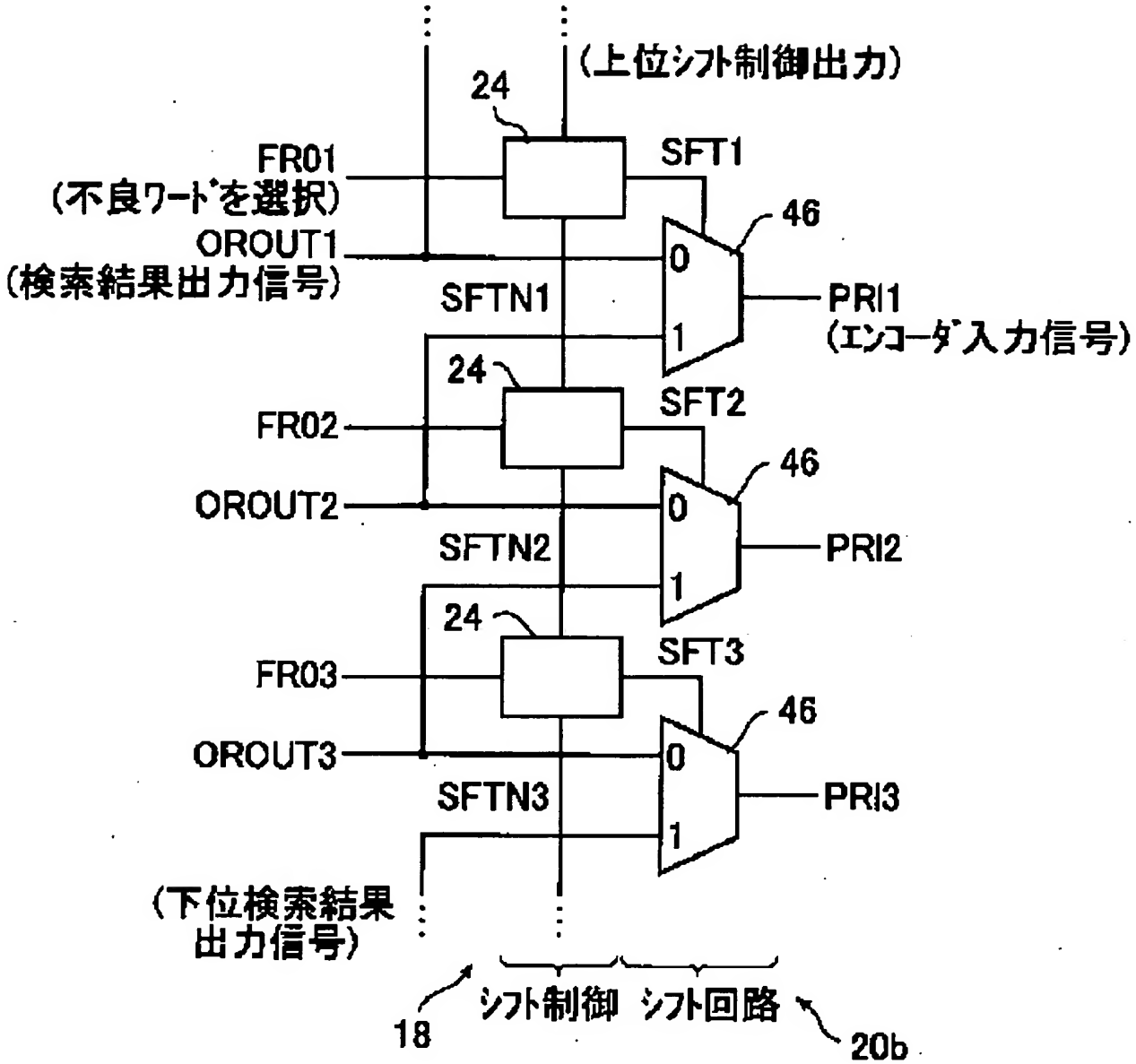

Logical
Physical
L0
L1
L2
L3
L4
L5
L6
P0
P1
P2
P3
P4
P5
P6
P7

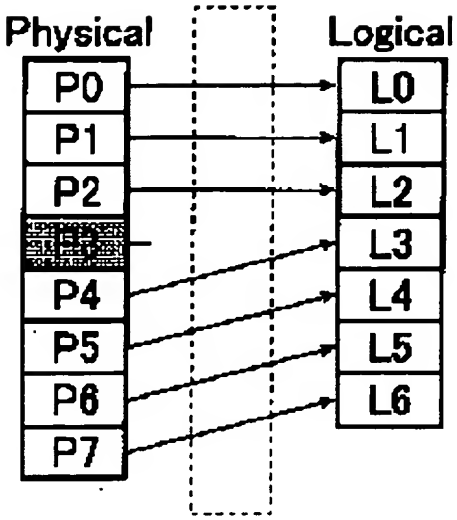
(a)


24
42
SFTN0
SW0
FAi,FBi,FCi,FDi
(プリデコード)
FRデコーダ
28
SFT1
GW1
30
SW1
GAi,GBi,GCi,GDi
(プリデコード)
W1
26
36
34
32
SFTN1
GW2
44
38
40
SW2
(プリデコード)
W2
44
GW3
シフト制御
シフト回路

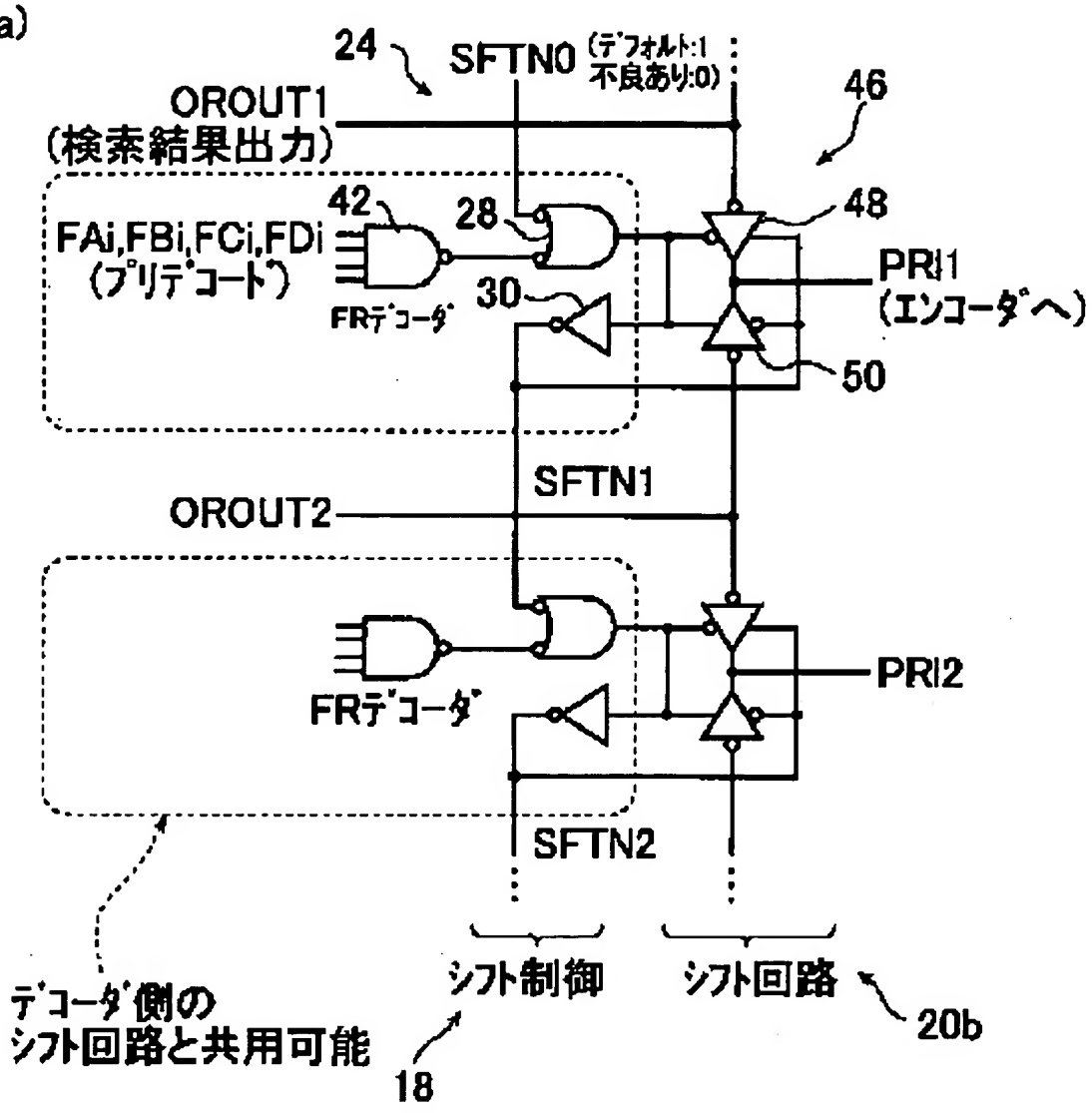
(b)


GAi,GBi,GCi,GDi
(プリデコード)
GWi
44
38
40

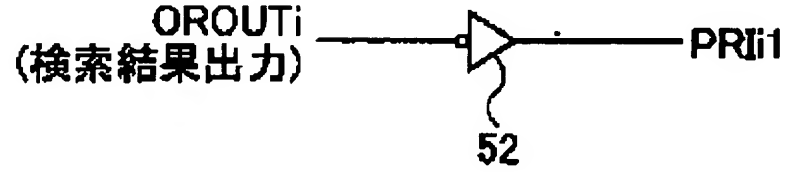

(上位シフト制御出力)
24
FR01
(不良ワードを選択)
SFT1
46
OROUT1
(検索結果出力信号)
0
SFTN1
PRI1
(エンコーダ入力信号)
1
24
SFT2
FR02
46
OROUT2
0
SFTN2
PRI2
1
24
SFT3
FR03
46
OROUT3
0
SFTN3
PRI3
1
(下位検索結果
出力信号)
18
シフト制御
シフト回路
20b

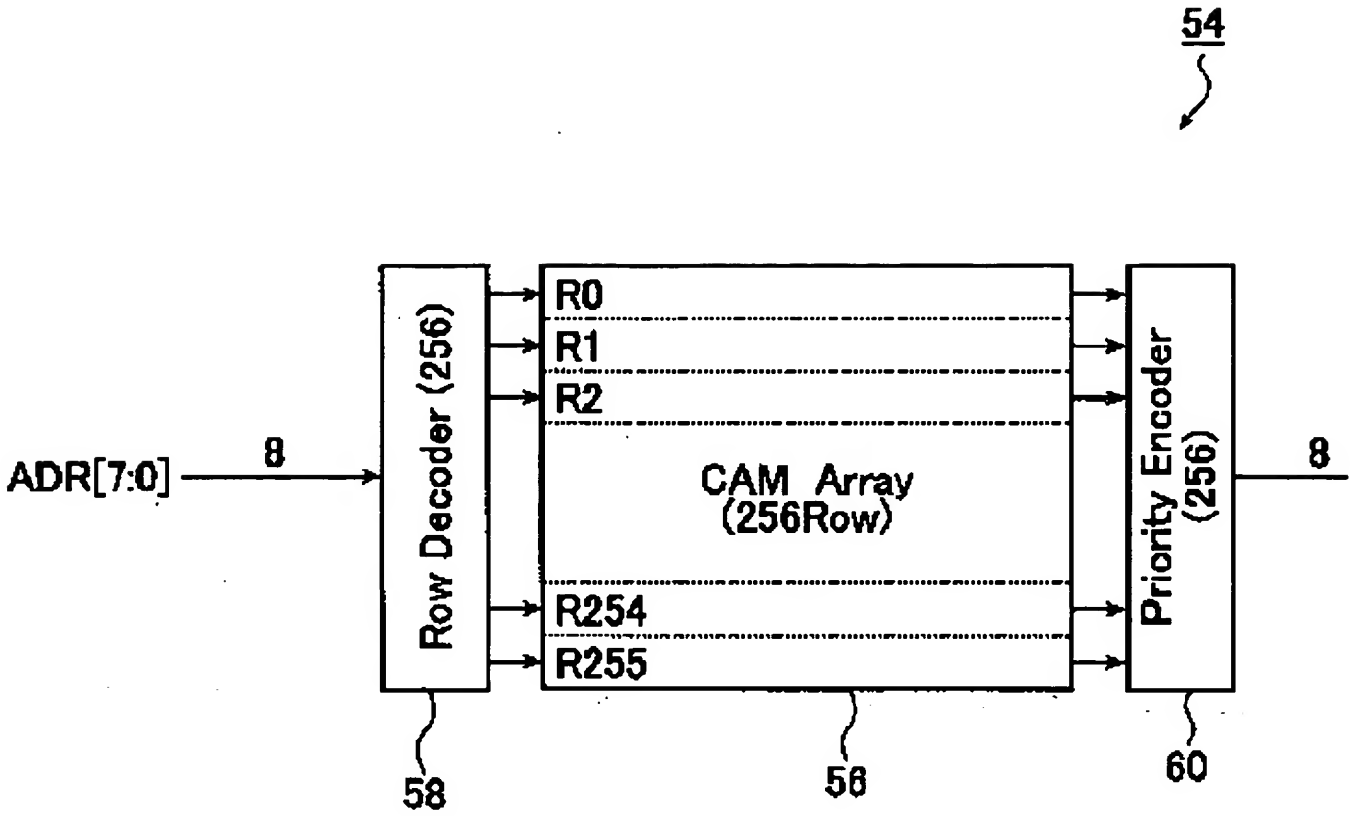

Physical
Logical
P0
P1
P2
P3
P4
P5
P6
P7
L0
L1
L2
L3
L4
L5
L6

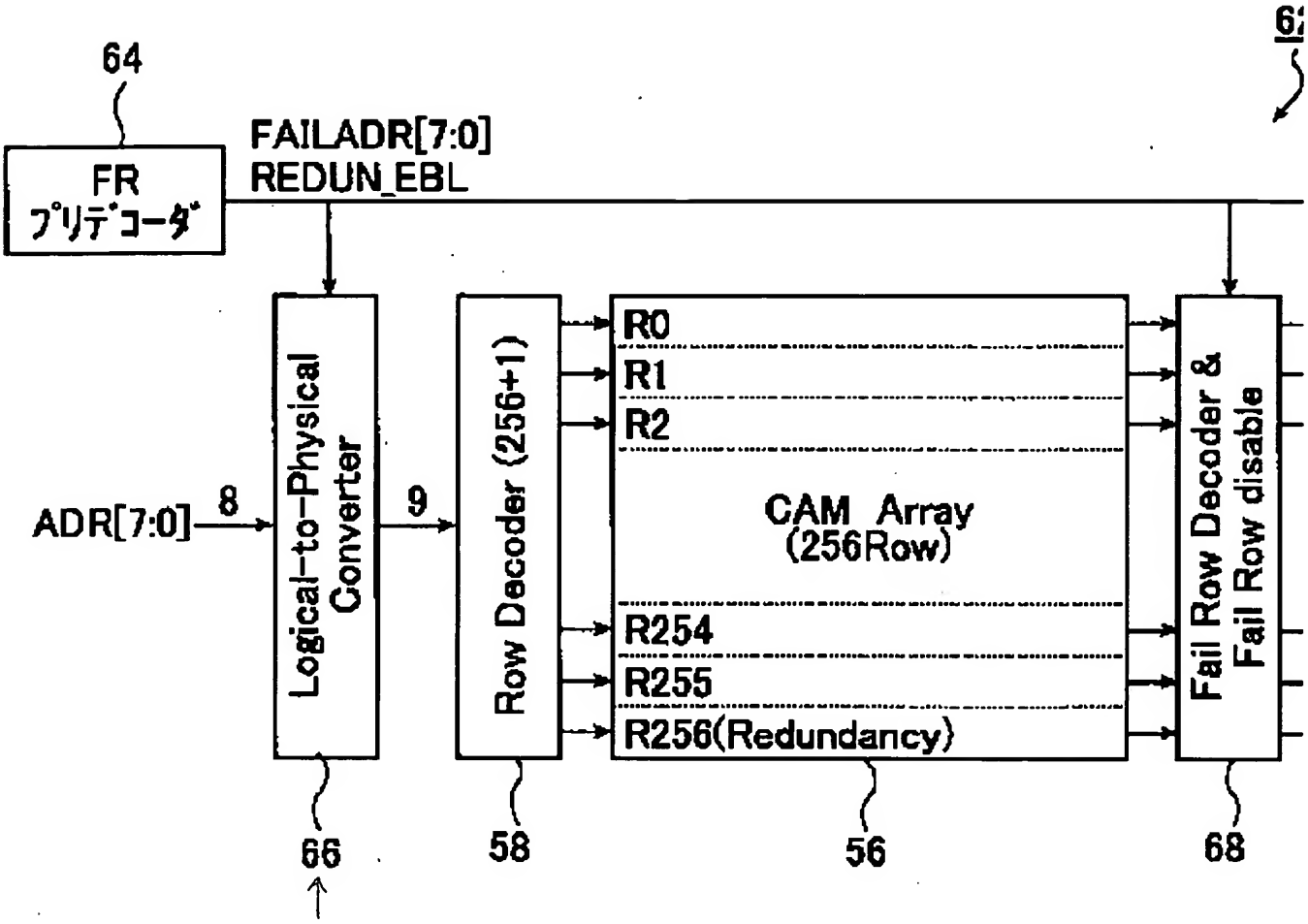
(a)


24
SFTN0
(デフォルト:1
不良あり:0)
46
OROUT1
(検索結果出力)
42
28
48
FAi,FBi,FCi,FDi
(プリデコード)
PRI1
(エンコーダへ)
30
FRデコーダ
50
SFTN1
OROUT2
PRI2
FRデコーダ
SFTN2
シフト制御
シフト回路
20b
デコーダ側の
シフト回路と共用可能
18

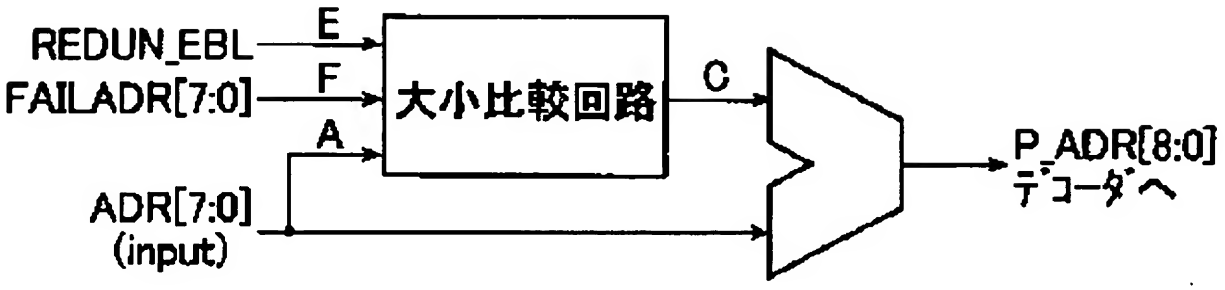
(b)


OROUTi
(検索結果出力)
PRIi1
52

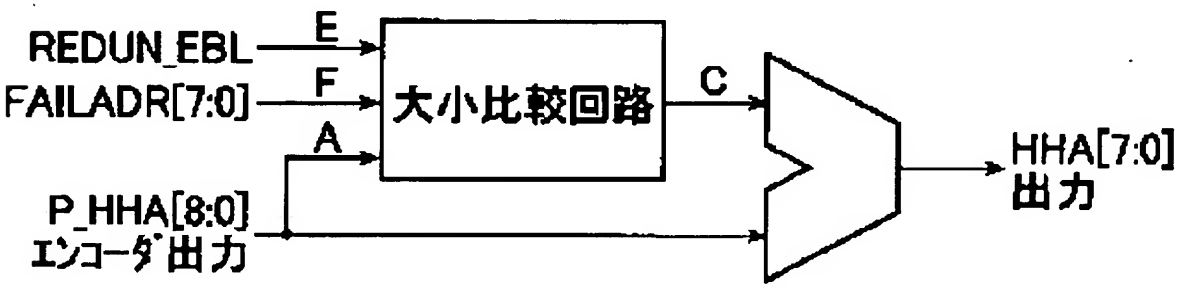

54
ADR[7:0]
8
Row Decoder (256)
R0
R1
R2
CAM Array
(256Row)
R254
R255
Priority Encoder
(256)
8
58
56
60

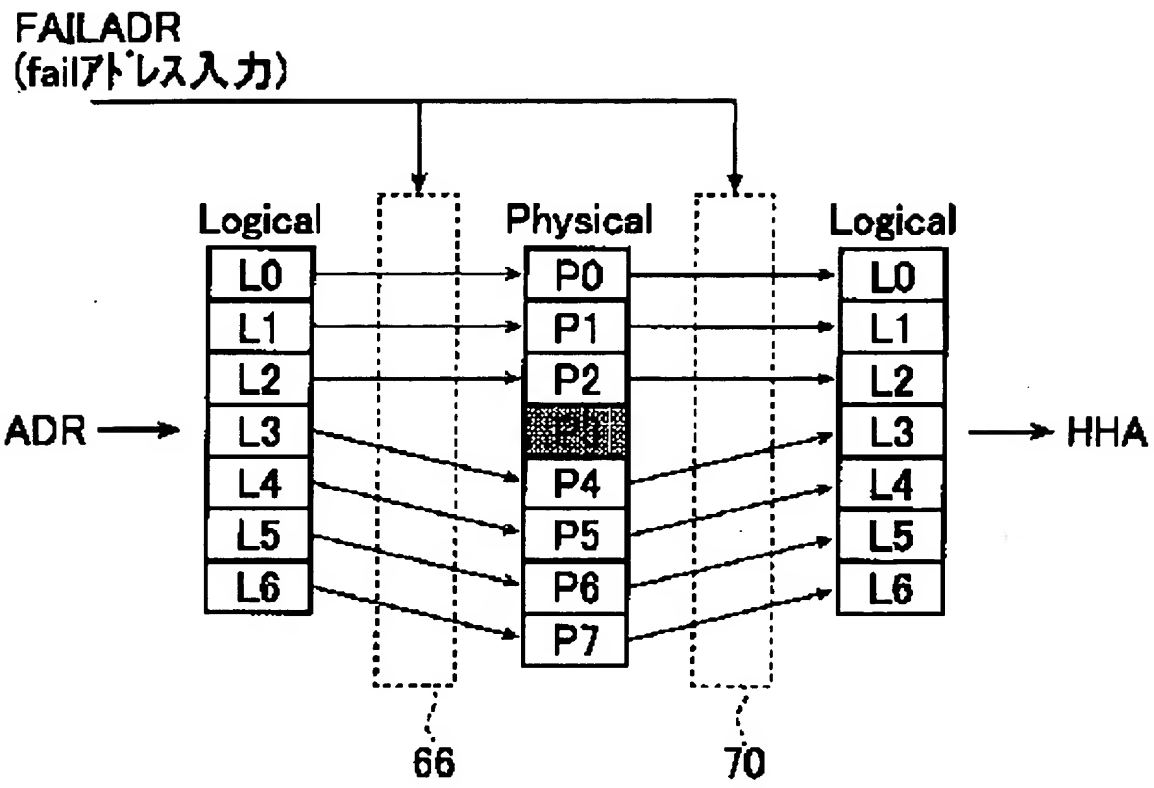

64
FR
ﾌﾟﾘﾃﾞｺｰﾀﾞ
FAILADR[7:0]
REDUN_EBL
ADR[7:0]
8
Logical-to-Physical Converter
9
Row Decoder (256+1)
R0
R1
R2
CAM Array (256Row)
R254
R255
R256(Redundancy)
Fail Row Decoder & Fail Row disable
66
58
56
68

(a)


REDUN_EBL
FAILADR[7:0]
ADR[7:0]
(input)
E
F
A
大小比較回路
C
P_ADR[8:0]
デコーダへ

(b)


REDUN_EBL
FAILADR[7:0]
P_HHA[8:0]
エンコーダ出力
E
F
A
大小比較回路
C
HHA[7:0]
出力


FAILADR
(failアドレス入力)
Logical
Physical
Logical
ADR
HHA
L0
L1
L2
L3
L4
L5
L6
P0
P1
P2
P3
P4
P5
P6
P7
66
70

TECHNICAL PROBLEM

[Problem(s) to be Solved by the Invention] however, in CAM62 using the conventional redundant circuit technology Since the logical address (address inputted from the outside) and the physical address (address actually used inside) are mutually changed using a size comparator circuit or an adder subtracter, The circuit scale becomes complicated large composition, and also the circuit 68 for forbidding the output of the memory address of poor CAM WORD is also needed, and expansion of the area by having added the redundant circuit serves as a big demerit.

[0017] Moreover, there is a problem that the time delay of an output increases remarkably compared with CAM54 in which the redundant circuit is not established since size comparison and addition and subtraction are performed each time, at the time of access of the read/write of stored data, and reference operation. Although this output time delay is based also on the circuitry of a size comparator circuit or an adder subtracter, 1 - 2ns or more and a bird clapper pose a **** and a big problem also concerning the spec. of CAM in especially the encoding output of the memory address after coincidence reference.

[0018] Without canceling the trouble based on the aforementioned conventional technology, and increasing a circuit scale and an output time delay, the purpose of this invention carries the CAM WORD of the reserve as a redundant circuit, and is to offer the associative memory which can raise the product yield.

TECHNICAL FIELD

[The technical field to which invention belongs] this invention relates to an associative memory (henceforth CAM (Content Addressable Memory)), and CAM equipped with the function to replace poor CAM WORD with spare CAM WORD, and to relieve it in more detail.

PRIOR ART

[Description of the Prior Art] Drawing 8 is the composition schematic diagram of an example of the conventional CAM. CAM54 shown in this drawing consists of a CAM array (CAM Array) 56 equipped with the CAM WORD for 256 word (256Row), a low decoder (Row Decoder) 58 which decodes address signal ADR [7:0], and a priority encoder (Priority Encoder) 60 which encodes the address of the CAM WORD by which coincidence was detected one by one according to predetermined priority.
[0003] In CAM54 of the example of illustration, the CAM WORD corresponding to address signal ADR [7:0] inputted from the outside is chosen by the low decoder 58, and access of the read/write of stored data is performed. Then, coincidence reference with the reference data inputted from the stored data memorized by each CAM WORD and the outside is performed simultaneously, and the memory address which is the CAM WORD by which coincidence was detected by the priority encoder 60 according to predetermined priority is outputted one by one.
[0004] By the way, in the usual semiconductor memory, such as SRAM (static RAM) and DRAM (dynamic RAM), when spare memory WORD is beforehand prepared as a redundant circuit and poor memory WORD exists, aid is given by replacing this poor memory WORD with spare memory WORD, and, generally the redundant circuit technology of raising the yield of semiconductor memory is used.
[0005] However, in CAM54, most relief of poor CAM WORD was not performed for the reasons of not only the address selection at the time of that the structure of the column differs from the usual semiconductor memory greatly, and access of the read/write of data (decoding) but functions peculiar to CAM54 -- aid must be given after coincidence reference also about the function (encoding) which outputs the coincidence address one by one according to priority -- circuitry, etc.
[0006] Hereafter, the redundant circuit technology of the conventional CAM is explained.
[0007] Drawing 9 is the composition schematic diagram of another example of the conventional CAM. CAM62 shown in this drawing applied redundant circuit technology, and is further equipped with FR pulley decoder 64, the logic-physics converter (Logical-to-Physical Converter) 66, a fail low decoder and the fail low disable (Fail Row Decoder & Fail Row disable) 68, and the physical - logic level converter (Physical-to-Logical Converter) 70 in CAM54 shown in drawing 8
[0008] The CAM array 56 is equipped with CAM WORD R256 of the reserve for 1 [besides usual CAM WORD R0, R1, R2, --, R255 for 256 word] word in CAM62 of the example of illustration. Moreover, when poor CAM WORD exists, address signal FAILADR [7:0] of this poor CAM WORD is remembered to be signal REDUN_EBL which means whether poor CAM WORD exists to FR pulley decoder 64.
[0009] First, in the logic-physics converter 66, when poor CAM WORD does not exist (signal REDUN_EBL=0), address signal ADR [7:0] is outputted as it is, and is inputted into the low decoder 58. On the other hand, when poor CAM WORD exists (signal REDUN_EBL=1), size comparison with address signal ADR [7:0] and address signal FAILADR [7:0] of poor CAM WORD which were inputted from the outside is performed.
[0010] Here, if it is ADR[7:0] >=FAILADR [7:0] as shown in drawing 10 (a), 1 will be added to address signal ADR [7:0], and it will be inputted into the low decoder 58 as signal P_ADR [8:0]. That is, every one memory address after the address of poor CAM WORD is carried down. On the other hand, if it is ADR[7:0] <FAILADR [7:0], address signal ADR [7:0] will be inputted into the low decoder 58 as it is.
[0011] In addition, operation of the low decoder 58, the CAM array 56, and a priority encoder 60 is the same as the case of CAM54 shown in drawing 8 except for the point that address signal P_ADR [8:0] is inputted from the logic-physics converter 66 instead of address signal ADR [7:0] being inputted from the exterior. Moreover, a fail low decoder and the fail low disable 68 cancel the detection result of the coincidence inequality outputted from poor CAM WORD.
[0012] Finally, in the physical - logic level converter 70, when poor CAM WORD does not exist (signal REDUN_EBL=0), address signal P_HHA [7:0] inputted from the priority encoder 60 is outputted as it is. On the other hand, when poor CAM WORD exists (signal REDUN_EBL=1), size comparison with

address signal P_HHA [8:0] and address signal FAILADR [7:0] of poor CAM WORD which were inputted from the priority encoder 60 is performed.
[0013] Here, if it is P_HHA[8:0] >=FAILADR [7:0] as shown in drawing 10 (b), from address signal ADR [7:0], 1 will be subtracted and it will be outputted as a signal HHA [7:0]. That is, every one memory address after the address of poor CAM WORD is advanced. On the other hand, if it is P_HHA [8:0] <FAILADR [7:0], address signal P_HHA [7:0] will be outputted as it is as a signal HHA [7:0].
[0014] That is, in CAM62, when the CAM WORD of P3 is poor CAM WORD as shown in drawing 11 for example, the memory address of P0-P2 is outputted for address signal ADR inputted from the outside as it is by the logic-physics converter 66, and every one memory address after P3 is carried down. Moreover, the memory address of P0-P2 is outputted as it is for the memory address after encoding by the physical - logic level converter 70, and every one memory address after P4 is advanced.

[0015] Therefore, a memory address is added if needed by the input side (decoder side) of an address signal, and by the external interface, CAM62 can be used by performing subtraction conversely at an output side (encoder side), without being completely conscious of existence of poor CAM WORD.

EFFECT OF THE INVENTION

[Effect of the Invention] As explained to the detail above, it replaces the reference coincidence output of spare CAM WORD, and the reference coincidence output of poor CAM WORD while the associative memory of this invention holds the address information of the poor CAM WORD contained in two or more CAM WORD, controls it according to the address information of this poor CAM WORD to replace poor CAM WORD and spare CAM WORD and replaces the address of poor CAM WORD, and the address of spare CAM WORD. Thereby, without increasing a circuit scale and an output time delay according to the associative memory of this invention, it can be used being able to replace poor CAM WORD and spare CAM WORD, and the yield of a product can be raised

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] It is the composition schematic diagram of one example of the associative memory of this invention.
[Drawing 2] It is the composition schematic diagram of one example of the shift circuit by the side of a decoder at the fail low decoder and shift control circuit row which are used by the associative memory of this invention.
[Drawing 3] It is the conceptual diagram of one example which expresses operation of the shift circuit by the side of a decoder to the fail low decoder and shift control circuit row which are shown in drawing 2 .
[Drawing 4] The component-circuit view of one example of the shift circuit by the side of a decoder and (b) are the component-circuit views of an example of the conventional low decoder at the low decoder, fail low decoder, and shift control circuit row for which (a) is used by the associative memory of this invention.
[Drawing 5] It is the composition schematic diagram of one example of the shift circuit by the side of an encoder at the fail low decoder and shift control circuit row which are used by the associative memory of this invention.
[Drawing 6] It is the conceptual diagram of one example which expresses operation of the shift circuit by the side of an encoder to the fail low decoder and shift control circuit row which are shown in drawing 5 .
[Drawing 7] The component-circuit view of one example of the shift circuit by the side of an encoder and (b) are the component-circuit views of an example of the output section by the side of the conventional encoder at the fail low decoder and shift control circuit row for which (a) is used by the associative memory of this invention.
[Drawing 8] It is the composition schematic diagram of an example of the conventional associative memory.
[Drawing 9] It is the composition schematic diagram of another example of the conventional associative memory.
[Drawing 10] The size comparator circuit for which (a) is used by the conventional associative memory and the composition schematic diagram of an example of an adder, and (b) are the size comparator circuit used by the conventional associative memory, and the composition schematic diagram of an example of a subtractor.
[Drawing 11] It is the conceptual diagram of an example showing operation of the conventional associative memory.
[Description of Notations]
10, 54, 62 Associative memory (CAM)
12 56 CAM array
14 58 Low decoder
16 64 FR pulley decoder
18 Fail Low Decoder and Shift Control Circuit
20a, 20b Shift circuit
22 60 Priority encoder
24 Control Circuit
26 46 Selector
28 OR Gate
30, 38, 52 Inverter
32 34 AND gate
36 NOR Gate
40 Buffer
42 44 NAND gate

48 50 Tri-state inverter
66 Logic-Physics Converter
68 Fail Low Decoder and Fail Low Disable
70 Physical-Logic Level Converter

MEANS

[Means for Solving the Problem] In order to attain the above-mentioned purpose, this invention is added to two or more CAM WORD. FR pulley decoder holding the address information of the poor CAM WORD which is the associative memory which carried the CAM WORD of the reserve as a redundant circuit, and is contained in two or more aforementioned CAM WORD, The CAM WORD of the aforementioned reserve is used according to the address information of the poor CAM WORD currently held at this FR pulley decoder. The 1st shift control circuit controlled to shift the address of the aforementioned CAM WORD by the side of the high order (or low rank) address rather than the aforementioned poor CAM WORD, At the time of access of the read/write of data, control of the shift control circuit of the above 1st is followed. The 1st shift circuit which shifts the i addresses of the aforementioned CAM WORD by the side of the high order (or low rank) address at a time to a high order (or low rank) address side rather than the aforementioned poor CAM WORD of eye i (i is one or more integers) watch, The CAM WORD of the aforementioned reserve is used according to the address information of the poor CAM WORD currently held at the aforementioned FR pulley decoder. The 2nd shift control circuit controlled to shift the address of the aforementioned CAM WORD by the side of the high order (or low rank) address rather than the aforementioned poor CAM WORD, At the time of reference operation, control of the shift control circuit of the above 2nd is followed. The associative memory characterized by having the 2nd shift circuit which shifts the i addresses of the aforementioned CAM WORD by the side of the high order (or low rank) address at a time to a low rank (or high order) address side rather than the i-th aforementioned poor CAM WORD is offered.

[0020] this invention to two or more CAM WORD Moreover, in addition, FR pulley decoder holding the address information of the poor CAM WORD which is the associative memory which carried the CAM WORD of the reserve as a redundant circuit, and is contained in two or more aforementioned CAM WORD, The CAM WORD of the aforementioned reserve is used according to the address information of the poor CAM WORD currently held at this FR pulley decoder. The shift control circuit controlled to shift the address of the aforementioned CAM WORD by the side of the high order (or low rank) address rather than the aforementioned poor CAM WORD, Control of the aforementioned shift control circuit is followed at the time of access of the read/write of data. The 1st shift circuit which shifts the i addresses of the aforementioned CAM WORD by the side of the high order (or low rank) address at a time to a high order (or low rank) address side rather than the aforementioned poor CAM WORD of eye i (i is one or more integers) watch, Control of the aforementioned shift control circuit is followed at the time of reference operation. The associative memory characterized by having the 2nd shift circuit which shifts the i addresses of the aforementioned CAM WORD by the side of the high order (or low rank) address at a time to a low rank (or high order) address side rather than the i-th aforementioned poor CAM WORD is offered.

[0021]

[Embodiments of the Invention] Below, based on the suitable example shown in an attached drawing, the associative memory of this invention is explained in detail.

[0022] Drawing 1 is the composition schematic diagram of one example of the associative memory of this invention. The associative memory (henceforth CAM) 10 shown in this drawing has the function to replace poor CAM WORD with the CAM WORD of the reserve as a redundant circuit, and to relieve it, and is equipped with the CAM array 12, the low decoder 14, FR pulley decoder 16, a fail low decoder and the shift control circuit 18, two shift circuits 20a and 20b, and priority encoders 22.

[0023] usual CAM WORD R0, R1, R2, --, R255 for 256 word (256Row) first specified in CAM10 of the example of illustration in the address which the CAM array (CAM Array) 12 followed -- in addition, it has CAM WORD (Redundancy) R256 of the redundant reserve for 1 word this example gives and explains the example which used the CAM array of the same composition so that comparison with CAM62 which applies the conventional redundant circuit shown in drawing 9 may become easy.

[0024] In addition, although this example explains noting that CAM WORD R0 is the CAM WORD of the most significant, it becomes low-ranking CAM WORD below at order in CAM WORD R1, R2, and

R3 and the order of -- and CAM WORD R255 is the CAM WORD of the least significant this invention may not be limited to this, but may make CAM WORD R0 the least significant, may make it the CAM WORD of a high order below at order in CAM WORD R1, R2, and R3 and the order of --, and may constitute the CAM array 12 for CAM WORD R255 as CAM WORD of the most significant.
[0025] Below, in order of, the low decoder (Row Decorder) 14 decodes the logical address [7:0], i.e., address signal ADR inputted from the outside, and outputs the WORD selection signal for specifying the CAM WORD corresponding to this. From the low decoder 14, 256 WORD selection signals respectively corresponding to CAM WORD R0, R1, R2, --, R255 are outputted, and let only one WORD selection signal corresponding to address signal ADR [7:0] be an active state.
[0026] FR pulley decoder 16 holds the address of this poor CAM WORD, when the information whether poor CAM WORD exists, and poor CAM WORD exist. From this FR pulley decoder 16, the signal FAILADR [7:0] in which the address of poor CAM WORD is expressed as signal REDUN_EBL showing whether poor CAM WORD exists is outputted.
[0027] The composition of this FR pulley decoder 16 constitute FR pulley decoder 16 using a fuse, and for example, by cutting a fuse according to the address of the corresponding poor CAM WORD May specify the memory address and Or the internal register is prepared, if it is a means by which the address of poor CAM WORD -- the address of poor CAM WORD may be stored in this internal register -- can be specified, it is not limited at all but each well-known means can use conventionally.
[0028] According to signal REDUN_EBL and Signal FAILADR [7:0], a fail low decoder and the shift control circuit (Fail Row Decoder & Shift Control) 18 use spare CAM WORD, and they output the shift control signal which controls operation of the shift circuits 20a and 20b so that the address of the CAM WORD by the side of the high order address may be shifted rather than poor CAM WORD. In this example, a shift control signal is inputted into both shift circuits 20a and 20b, and the fail low decoder and the shift control circuit 18 are shared in the shift circuits 20a and 20b.
[0029] Shift circuit (Shift Circuit) 20a by the side of a decoder [whether according to control of a shift control signal, 256 WORD selection signals inputted through a fail low decoder and the shift control circuit 18 from the low decoder 14 are outputted as they are, and] Or every one WORD selection signal corresponding to all the CAM WORD by the side of the low rank address is shifted to the CAM WORD by the side of the low rank address rather than poor CAM WORD. That is, the address of all the CAM WORD by the side of the low rank address is shifted to a low rank address side rather than poor CAM WORD.
[0030] On the other hand, shift circuit 20b by the side of an encoder [whether similarly, 256 reference coincidence output signals by the side of the high order address of the 257 reference coincidence output signals inputted through a coincidence line by control of a shift control signal from each CAM WORD of the CAM array 12 are outputted as they are, and] Or every one reference coincidence output signal corresponding to all the CAM WORD by the side of the low rank address is shifted to the CAM WORD by the side of the high order address rather than poor CAM WORD. That is, the address of all the CAM WORD by the side of the low rank address is shifted to a high order address side rather than poor CAM WORD.
[0031] Here, when poor CAM WORD does not exist (signal REDUN_EBL=0), it is controlled so that the logical address and the physical address which are CAM WORD are in agreement. That is, 256 WORD selection signals outputted from the low decoder 14 are inputted into CAM WORD R0, R1, R2, --, R255 which corresponds respectively as they are, and the reference coincidence output signal outputted from CAM WORD R0, R1, R2, --, R255 is also inputted into a priority encoder 22 as it is.
[0032] On the other hand, when poor CAM WORD exists (signal REDUN_EBL=1), according to Signal FAILADR [7:0], every one WORD selection signal corresponding to all the CAM WORD by the side of the low rank address is shifted to the CAM WORD by the side of the low rank address rather than poor CAM WORD. Moreover, every one reference coincidence output signal corresponding to all the CAM WORD by the side of the low rank address is shifted to the CAM WORD by the side of the high order address rather than poor CAM WORD.
[0033] Finally, about 256 reference coincidence output signals inputted from shift circuit 20b, according

to predetermined priority, a priority encoder (Priority Encoder) 22 encodes the memory address which is the CAM WORD by which coincidence was detected one by one, and outputs this one by one as the ranking hit address HHA of the highest priority [7:0]. Though it is not limited at all, for example, the priority of CAM WORD has so high that it is the CAM WORD by the side of the low rank address or the high order address priority, it is good.
[0034] In addition, neither the number of WORD of a CAM array nor the number of bits of the CAM cell contained in 1 word is limited at all. Moreover, although it could be prepared what word and is arranged to the memory address by the side of the least significant in the example of illustration, even if it arranges to the memory address by the side of the most significant or arranges spare CAM WORD to other memory addresses, it is easy to be natural [WORD]. Moreover, each thing of well-known composition can use the low decoder 14 and a priority encoder 22 conventionally.
[0035] When the CAM WORD of two or more reserves is prepared, here in shift circuit 20a by the side of a decoder Every one address of the CAM WORD by the side of the low rank address is shifted to a low rank address side rather than the 1st poor CAM WORD. Every two addresses of the CAM WORD by the side of the low rank address are shifted to a low rank address side rather than the 2nd poor CAM WORD. It is necessary to shift the i addresses of the CAM WORD by the side of the low rank address at a time to a low rank address side like the following rather than the poor CAM WORD of eye i (i is one or more integers) watch.
[0036] When the CAM WORD of two or more reserves is prepared, moreover, in shift circuit 20b by the side of an encoder Every one address of the CAM WORD by the side of the low rank address is shifted to a high order address side rather than the 1st poor CAM WORD. It is necessary to shift every two addresses of the CAM WORD by the side of the low rank address to a high order address side rather than the 2nd poor CAM WORD, and to shift the i addresses of the CAM WORD by the side of the low rank address at a time to a high order address side rather than the i-th poor CAM WORD like the following.
[0037] Next, two shift circuits 20a and 20b are explained more to the fail low decoder shown in drawing 1 and the shift control circuit 18, and a row at a detail.
[0038] Drawing 2 is the composition schematic diagram of one example of the shift circuit by the side of a decoder at the fail low decoder and shift control circuit row which are used by the associative memory of this invention. As shown in this drawing, the fail low decoder and the shift control circuit 18 are equipped with the control circuit 24 prepared respectively corresponding to the poor CAM WORD selection signal. Moreover, shift circuit 20a by the side of a decoder is equipped with the selector 26 prepared corresponding to each CAM WORD R0, R1, R2, --, R256.
[0039] Here, the reversal signal SFTNi of the poor CAM WORD selection signal FRi which corresponds respectively, and the shift control signal outputted from the control circuit (control circuit corresponding to the poor CAM WORD selection signal by the side of the 1-word high order address) 24 of the preceding paragraph is inputted into each control circuit 24 of a fail low decoder and the shift control circuit 18. Moreover, the shift control signal SFTi outputted from each control circuit 24 is inputted into the selection terminal of a selector 26 with which shift circuit 20a corresponds respectively.

[0040] In addition, the poor CAM WORD selection signal FRi is a signal which decodes the signal FAILADR showing the address of poor CAM WORD [7:0], and is acquired. When all the poor CAM WORD selection signals FRi are inactive when, as for the poor CAM WORD selection signal FRi, poor CAM WORD does not exist in the case of this example, on the other hand poor CAM WORD exists, only one poor CAM WORD selection signal FRi will be in an active state.
[0041] Moreover, WORD selection-signal Wi-1 corresponding to the CAM WORD by the side of 1 high order address is inputted into each selector 26 of shift circuit 20a as the WORD selection signal Wi corresponding to each CAM WORD R0, R1, R2, --, R256. Moreover, the shift control signal SFTi is inputted into the selection terminal of each selector 26 from the control circuit 24 which corresponds respectively as above-mentioned, and the output signal GWi of each selector 26 is inputted into the CAM WORD which corresponds respectively.

[0042] In a fail low decoder and the shift control circuit 18, when poor CAM WORD does not exist, the shift control signal SFTi outputted from each control circuit 24 is inactive. According to this, the WORD selection signal Wi corresponding to each CAM WORD Ri is outputted from each selector 26 as a WORD signal GWi by shift circuit 20a.
[0043] On the other hand, when poor CAM WORD exists, the shift control signal SFTi outputted from the control circuit 24 corresponding to all the poor CAM WORD selection signals FRi by the side of the low rank address containing the poor CAM WORD selection signal FRi of an active state will be in an active state. According to this, WORD selection-signal Wi-1 corresponding to the CAM WORD by the side of 1 high order address is outputted as a WORD signal GWi from each selector 26.
[0044] That is, as shown intelligibly for the conceptual diagram of drawing 3 , there is the usual CAM WORD to P0-P6, and it presupposes that there is P7 which is spare CAM WORD. Here, supposing poor CAM WORD is P3, the WORD selection signals L0-L2 which correspond respectively will be inputted into CAM WORD P0-P2. Poor CAM WORD P3 is fixed to a low level, and the WORD selection signals L3-L6 respectively shifted one [at a time] are inputted into CAM WORD P4-P7.
[0045] Here, the example shown in drawing 4 is given and the shift circuit by the side of a decoder is further explained to a fail low decoder and a shift control circuit row at a detail.
[0046] As shown in drawing 4 (a), each control circuit 24 of a fail low decoder and the shift control circuit 18 consists of the OR gate 28 and an inverter 30. The reversal signal SFTNi of the poor CAM WORD selection signal which corresponds respectively, and the shift control signal outputted from the control circuit 24 of the preceding paragraph is inputted into two inversed input terminals of the OR gate 28. Moreover, from the OR gate 28, the shift control signal SFTi is outputted and the reversal signal SFTNi is outputted through the inverter 30.
[0047] Moreover, each selector 26 of shift circuit 20a by the side of a decoder consists of the two AND gates 32 and 34, the NOR gates 36, inverters 38, and buffers 40. The WORD selection signal Wi corresponding to each CAM WORD Ri and the shift control signal SFTi outputted from the OR gate 28 of a control circuit 24 which corresponds respectively are inputted into two inversed input terminals of the AND gate 34. On the other hand, WORD selection-signal Wi-1 corresponding to CAM WORD Ri-1 by the side of 1 high order address and reversal signal SFTNi-1 of the shift control signal outputted from the inverter 30 of the control circuit 24 of the preceding paragraph are inputted into two inversed input terminals of the AND gate 32. Moreover, both the output signals of the AND gates 32 and 34 are inputted into the NOR gate 36, and the output signal of the NOR gate 36 is outputted as a WORD signal GWi through the inverter 38 and the buffer 40.
[0048] When poor CAM WORD does not exist in the circuit shown in drawing 4 (a), in the poor CAM WORD selection signal and the example of illustration which decode Signal FAILADR [7:0] and are acquired, all the output signals of NAND gate 42 become high-level. Moreover, when poor CAM WORD does not exist, the reversal signal SFTN0 of the shift control signal of the most-significant address is high-level, and, in the output signal SFTi of the OR gate 28, i.e., all shift control signals, a low level and the output signal SFTNi of an inverter 30, i.e., the reversal signal of a shift control signal, become high-level altogether.
[0049] Therefore, since the output signal of the AND gate 32 into which the reversal signal SFTNi of a shift control signal is inputted serves as a low level, the WORD selection signal Wi outputted from the low decoder 14 is outputted from the AND gate 34 into which the shift control signal SFTi is inputted, and it is outputted as a WORD signal GWi through the NOR gate 36, an inverter 38, and a buffer 40.
[0050] On the other hand, when poor CAM WORD exists, only the poor CAM WORD selection signal which decodes Signal FAILADR [7:0] and is obtained serves as a low level. Thereby, the shift control signal SFTi corresponding to all the CAM WORD by the side of the low rank address containing this poor CAM WORD selection signal FRi becomes high-level, and the reversal signal SFTNi serves as a low level altogether.
[0051] therefore, in the selector 26 corresponding to all the CAM WORD by the side of the low rank address containing the poor CAM WORD selection signal of a low level Since the output signal of the AND gate 34 into which the shift control signal SFTi is inputted serves as a low level Are outputted

from the AND gate 32 into which the reversal signal SFTNi is inputted to the low decoder 14. WORD selection-signal Wi-1 corresponding to the CAM WORD by the side of 1 high order address is outputted, and it is outputted as a WORD signal GWi through the NOR gate 36, an inverter 38, and a buffer 40.

[0052] In addition, in the selector 26 corresponding to all the CAM WORD by the side of the high order address, the shift control signal SFTi serves as a low level, and the reversal signal SFTNi is still altogether more high-level than the poor CAM WORD selection signal of a low level. Therefore, by the selector 26 corresponding to all the CAM WORD by the side of the high order address, it operates completely like the case where poor CAM WORD does not exist, rather than the poor CAM WORD selection signal of a low level.

[0053] Drawing 4 (b) is the component-circuit view of an example of the conventional low decoder. This drawing shows a part for 1 word of the low decoder used by the conventional CAM which has not applied redundant circuit technology, in order to make intelligible the scale of the additional circuit concerning this invention. Here, NAND gate 44, an inverter 38, and a buffer 40 are equivalent to NAND gate 44, an inverter 38, and a buffer 40 in the circuit concerning this invention shown in drawing 4 (a), respectively.

[0054] The additional portions of the circuit concerning this invention are only the OR gate 28 and the inverter 30 equivalent to a control circuit 24, and the two AND gates 32 and 34 and the NOR gate 36 equivalent to a selector 26 so that clearly, if the circuit shown in this drawing 4 (a) and (b) is compared. These circuits are circuits added to the conventional CAM shown in drawing 8 , if compared with the additional circuit in the conventional CAM shown in drawing 9 , the circuit scale is extraordinarily small and the output time delay is also very short.

[0055] Then, drawing 5 is the composition schematic diagram of one example of the shift circuit by the side of an encoder at the fail low decoder and shift control circuit row which are used by the associative memory of this invention. As shown in this drawing, the composition of a fail low decoder and the shift control circuit 18 is the same as that of what is shown in drawing 2 . Moreover, shift circuit 20b by the side of an encoder is equipped with the selector 46 prepared corresponding to each CAM WORD R0, R1, R2, --, R255.

[0056] In addition, in the example shown in drawing 5 , in order to make an understanding easy, the fail low decoder and the shift control circuit 18 are formed also in the preceding paragraph of shift circuit 20b by the side of an encoder. Thus, the shift control signal SFTi and its reversal signal SFTNi are taken about, a fail low decoder and the shift control circuit 18 connect, and you may make it share a fail low decoder and the shift control circuit 18 in both, as you may prepare in the shift circuits 20a and 20b by the side of a decoder and an encoder individually, respectively and it is shown in drawing 1 .

[0057] In shift circuit 20b shown in drawing 5 , reference result output signal OROUTi+1 corresponding to the CAM WORD by the side of the reference result output signal OROUTi corresponding to each CAM WORD R0, R1, R2, --, R256 and 1 low rank address is inputted into each selector 46. Moreover, the shift control signal SFTi which corresponds respectively is inputted into the selection terminal of each selector 46, and the output signal PRli of each selector 46 is inputted into the priority encoder 22.

[0058] Operation of a fail low decoder and the shift control circuit 18 is as above-mentioned. That is, when poor CAM WORD does not exist, the shift control signal SFTi outputted from each control circuit 24 is inactive. According to this, the reference result output signal OROUTi corresponding to each CAM WORD Ri is outputted from each selector 46 as a signal PRli by shift circuit 20b.

[0059] On the other hand, when poor CAM WORD exists, the shift control signal SFTi outputted from the control circuit 24 corresponding to all the poor CAM WORD selection signals FRi by the side of the low rank address containing the poor CAM WORD selection signal FRi of an active state will be in an active state. According to this, reference result output signal OROUTi+1 corresponding to the CAM WORD by the side of 1 low rank address is outputted as a signal PRli from each selector 46.

[0060] That is, as shown intelligibly for the conceptual diagram of drawing 6 , there is the same usual CAM WORD to P0-P6, there is P7 which is spare CAM WORD, and supposing poor CAM WORD is P3, the reference result output signal of CAM WORD P0-P2 will be outputted as signals L0-L2 as it is.

Moreover, the reference result output signal of CAM WORD P3 is disregarded, and every one reference result output signal of CAM WORD P4-P7 is shifted respectively, and is outputted as signals L3-L6.
[0061] Here, the example shown in drawing 7 is given and the shift circuit by the side of a decoder is further explained to a fail low decoder and a shift control circuit row at a detail.
[0062] As shown in drawing 7 (a), each control circuit 24 of a fail low decoder and the shift control circuit 18 is completely the same as what is shown in drawing 4 (a). Therefore, as already stated, the portion surrounded with the dashed line of drawing 7 (a) can be used with shift circuit 20a by the side of a decoder in common, and as shown in drawing 1 , from a fail low decoder and the shift control circuit 18, the shift control signal SFTi and its reversal signal SFTNi may be taken about, and it may connect.
[0063] Moreover, each selector 46 of shift circuit 20b by the side of an encoder is constituted by two tri-state inverters 48 and 50. The reference result output OROUTi of the CAM WORD which corresponds respectively is inputted into the tri-state inverter 48, reference result output OROUTi+1 of the CAM WORD by the side of 1 low rank address is inputted, wye yard connection is made and both output signal is outputted to the tri-state inverter 50 as a signal PRli.
[0064] Moreover, the shift control signal SFTi (output signal of the OR gate 28) which corresponds respectively is inputted into the control inversed input terminal of the tri-state inverter 48, and the control-input terminal of the tri-state inverter 50, and the reversal signal SFTNi of the shift control signal which corresponds respectively is inputted into the control-input terminal of the tri-state inverter 48, and the control inversed input terminal of the tri-state inverter 50. That is, according to the state of the shift control signal SFTi and its reversal signal SFTNi, only either turns off ON and another side.
[0065] In the circuit shown in drawing 7 (a), when poor CAM WORD does not exist, as already stated, in all poor CAM WORD selection signals and examples of illustration, all the output signals of NAND gate 42 become high-level. Moreover, the reversal signal SFTN0 of the shift control signal of the most-significant address is high-level, and, in the output signal SFTi of the OR gate 28, i.e., all shift control signals, a low level and the output signal SFTNi of an inverter 30, i.e., the reversal signal of a shift control signal, become high-level altogether.
[0066] Therefore, the tri-state inverter 48 as which the reversal signal SFTNi of a shift control signal is inputted into the control-input terminal turns on, and since the tri-state inverter 50 as which the shift control signal SFTi is inputted into the control-input terminal turns off, the reference result output OROUTi of the CAM WORD which corresponds respectively is outputted as a signal PRli.
[0067] On the other hand, when poor CAM WORD exists, as similarly stated already, only the poor CAM WORD selection signal (output signal of a NAND gate) which decodes Signal FAILADR [7:0] and is obtained serves as a low level. Thereby, the shift control signal SFTi corresponding to all the CAM WORD by the side of the low rank address containing this poor CAM WORD selection signal FRi becomes high-level, and the reversal signal SFTNi serves as a low level altogether.
[0068] Therefore, in the selector 46 corresponding to all the CAM WORD by the side of the low rank address containing the poor CAM WORD selection signal of a low level, the tri-state inverter 50 as which the shift control signal SFTi is inputted into the control-input terminal turns on, and since the tri-state inverter 48 as which the reversal signal SFTNi of a shift control signal is inputted into the control-input terminal turns off, reference result output OROUTi+1 of the CAM WORD by the side of 1 low rank address is outputted as a signal PRli.
[0069] In addition, in the selector 46 corresponding to all the CAM WORD by the side of the high order address, the shift control signal SFTi serves as a low level, and the reversal signal SFTNi is still altogether more high-level than the poor CAM WORD selection signal of a low level. Therefore, by the selector 46 corresponding to all the CAM WORD by the side of the high order address, it operates completely like the case where poor CAM WORD does not exist, rather than the poor CAM WORD selection signal of a low level.
[0070] Drawing 7 (b) is the component-circuit view of an example of the output section by the side of the conventional encoder. This drawing shows a part for the output section by the side of the encoder used by the conventional CAM which has not applied redundant circuit technology, i.e., 1 word of the reference result output of each CAM WORD, in order to make intelligible the scale of the additional

circuit concerning this invention. Here, an inverter 52 is equivalent to the tri-state inverter 48 in the circuit concerning this invention shown in drawing 7 (a).

[0071] Supposing the additional portion of the circuit concerning this invention shares the circuit portion equivalent to a control circuit 24, it is only the tri-state inverter 50 which constitutes a selector 46, so that clearly, if the circuit shown in this drawing 7 (a) and (b) is compared. This circuit is a circuit added to the conventional CAM shown in drawing 8 , if compared with the additional circuit in the conventional CAM shown in drawing 9 , the circuit scale is extraordinarily small and the output time delay is also very short.

[0072] As mentioned above, in CAM of this invention, the scale of the circuit which changes mutually the logical address (address inputted from the outside) and a physical address (address actually used inside) is small. and since neither size comparison nor addition and subtraction is necessarily performed each time at the time of access of the read/write of stored data, and reference operation unlike CAM using the redundant circuit technology of the conventional method, even if it compares with the conventional CAM in which the redundant circuit is not established, an output time delay is an EQC mostly

[0073] The associative memory of this invention is fundamentally above. As mentioned above, although the associative memory of this invention was explained in detail, of course in the range which this invention is not limited to the above-mentioned example, and does not deviate from the main point of this invention, you may make various improvement and change.

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[The technical field to which invention belongs] this invention relates to an associative memory (henceforth CAM (Content Addressable Memory)), and CAM equipped with the function to replace poor CAM WORD with spare CAM WORD, and to relieve it in more detail.
[0002]
[Description of the Prior Art] Drawing 8 is the composition schematic diagram of an example of the conventional CAM. CAM54 shown in this drawing consists of a CAM array (CAM Array) 56 equipped with the CAM WORD for 256 word (256Row), a low decoder (Row Decoder) 58 which decodes address signal ADR [7:0], and a priority encoder (Priority Encoder) 60 which encodes the address of the CAM WORD by which coincidence was detected one by one according to predetermined priority.
[0003] In CAM54 of the example of illustration, the CAM WORD corresponding to address signal ADR [7:0] inputted from the outside is chosen by the low decoder 58, and access of the read/write of stored data is performed. Then, coincidence reference with the reference data inputted from the stored data memorized by each CAM WORD and the outside is performed simultaneously, and the memory address which is the CAM WORD by which coincidence was detected by the priority encoder 60 according to predetermined priority is outputted one by one.
[0004] By the way, in the usual semiconductor memory, such as SRAM (static RAM) and DRAM (dynamic RAM), when spare memory WORD is beforehand prepared as a redundant circuit and poor memory WORD exists, aid is given by replacing this poor memory WORD with spare memory WORD, and, generally the redundant circuit technology of raising the yield of semiconductor memory is used.
[0005] However, in CAM54, most relief of poor CAM WORD was not performed for the reasons of not only the address selection at the time of that the structure of the column differs from the usual semiconductor memory greatly, and access of the read/write of data (decoding) but functions peculiar to CAM54 -- aid must be given after coincidence reference also about the function (encoding) which outputs the coincidence address one by one according to priority -- circuitry, etc.
[0006] Hereafter, the redundant circuit technology of the conventional CAM is explained.
[0007] Drawing 9 is the composition schematic diagram of another example of the conventional CAM. CAM62 shown in this drawing applied redundant circuit technology, and is further equipped with FR pulley decoder 64, the logic-physics converter (Logical-to-Physical Converter) 66, a fail low decoder and the fail low disable (Fail Row Decoder & Fail Row disable) 68, and the physical - logic level converter (Physical-to-Logical Converter) 70 in CAM54 shown in drawing 8
[0008] The CAM array 56 is equipped with CAM WORD R256 of the reserve for 1 [besides usual CAM WORD R0, R1, R2, --, R255 for 256 word] word in CAM62 of the example of illustration. Moreover, when poor CAM WORD exists, address signal FAILADR [7:0] of this poor CAM WORD is remembered to be signal REDUN_EBL which means whether poor CAM WORD exists to FR pulley decoder 64.
[0009] First, in the logic-physics converter 66, when poor CAM WORD does not exist (signal REDUN_EBL=0), address signal ADR [7:0] is outputted as it is, and is inputted into the low decoder 58. On the other hand, when poor CAM WORD exists (signal REDUN_EBL=1), size comparison with address signal ADR [7:0] and address signal FAILADR [7:0] of poor CAM WORD which were inputted from the outside is performed.
[0010] Here, if it is ADR[7:0] >=FAILADR [7:0] as shown in drawing 10 (a), 1 will be added to address signal ADR [7:0], and it will be inputted into the low decoder 58 as signal P_ADR [8:0]. That is, every one memory address after the address of poor CAM WORD is carried down. On the other hand, if it is ADR[7:0] <FAILADR [7:0], address signal ADR [7:0] will be inputted into the low decoder 58 as it is.
[0011] In addition, operation of the low decoder 58, the CAM array 56, and a priority encoder 60 is the same as the case of CAM54 shown in drawing 8 except for the point that address signal P_ADR [8:0] is inputted from the logic-physics converter 66 instead of address signal ADR [7:0] being inputted from

the exterior. Moreover, a fail low decoder and the fail low disable 68 cancel the detection result of the coincidence inequality outputted from poor CAM WORD.
[0012] Finally, in the physical - logic level converter 70, when poor CAM WORD does not exist (signal REDUN_EBL=0), address signal P_HHA [7:0] inputted from the priority encoder 60 is outputted as it is. On the other hand, when poor CAM WORD exists (signal REDUN_EBL=1), size comparison with address signal P_HHA [8:0] and address signal FAILADR [7:0] of poor CAM WORD which were inputted from the priority encoder 60 is performed.
[0013] Here, if it is P_HHA[8:0] >=FAILADR [7:0] as shown in drawing 10 (b), from address signal ADR [7:0], 1 will be subtracted and it will be outputted as a signal HHA [7:0]. That is, every one memory address after the address of poor CAM WORD is advanced. On the other hand, if it is P_HHA [8:0] <FAILADR [7:0], address signal P_HHA [7:0] will be outputted as it is as a signal HHA [7:0].
[0014] That is, in CAM62, when the CAM WORD of P3 is poor CAM WORD as shown in drawing 11 for example, the memory address of P0-P2 is outputted for address signal ADR inputted from the outside as it is by the logic-physics converter 66, and every one memory address after P3 is carried down. Moreover, the memory address of P0-P2 is outputted as it is for the memory address after encoding by the physical - logic level converter 70, and every one memory address after P4 is advanced.

[0015] Therefore, a memory address is added if needed by the input side (decoder side) of an address signal, and by the external interface, CAM62 can be used by performing subtraction conversely at an output side (encoder side), without being completely conscious of existence of poor CAM WORD.
[0016]
[Problem(s) to be Solved by the Invention] however, in CAM62 using the conventional redundant circuit technology Since the logical address (address inputted from the outside) and the physical address (address actually used inside) are mutually changed using a size comparator circuit or an adder subtracter, The circuit scale becomes complicated large composition, and also the circuit 68 for forbidding the output of the memory address of poor CAM WORD is also needed, and expansion of the area by having added the redundant circuit serves as a big demerit.
[0017] Moreover, there is a problem that the time delay of an output increases remarkably compared with CAM54 in which the redundant circuit is not established since size comparison and addition and subtraction are performed each time, at the time of access of the read/write of stored data, and reference operation. Although this output time delay is based also on the circuitry of a size comparator circuit or an adder subtracter, 1 - 2ns or more and a bird clapper pose a **** and a big problem also concerning the spec. of CAM in especially the encoding output of the memory address after coincidence reference.
[0018] Without canceling the trouble based on the aforementioned conventional technology, and increasing a circuit scale and an output time delay, the purpose of this invention carries the CAM WORD of the reserve as a redundant circuit, and is to offer the associative memory which can raise the product yield.
[0019]
[Means for Solving the Problem] In order to attain the above-mentioned purpose, this invention is added to two or more CAM WORD. FR pulley decoder holding the address information of the poor CAM WORD which is the associative memory which carried the CAM WORD of the reserve as a redundant circuit, and is contained in two or more aforementioned CAM WORD, The CAM WORD of the aforementioned reserve is used according to the address information of the poor CAM WORD currently held at this FR pulley decoder. The 1st shift control circuit controlled to shift the address of the aforementioned CAM WORD by the side of the high order (or low rank) address rather than the aforementioned poor CAM WORD, At the time of access of the read/write of data, control of the shift control circuit of the above 1st is followed. The 1st shift circuit which shifts the i addresses of the aforementioned CAM WORD by the side of the high order (or low rank) address at a time to a high order (or low rank) address side rather than the aforementioned poor CAM WORD of eye i (i is one or more integers) watch, The CAM WORD of the aforementioned reserve is used according to the address information of the poor CAM WORD currently held at the aforementioned FR pulley decoder. The 2nd

shift control circuit controlled to shift the address of the aforementioned CAM WORD by the side of the high order (or low rank) address rather than the aforementioned poor CAM WORD, At the time of reference operation, control of the shift control circuit of the above 2nd is followed. The associative memory characterized by having the 2nd shift circuit which shifts the i addresses of the aforementioned CAM WORD by the side of the high order (or low rank) address at a time to a low rank (or high order) address side rather than the i-th aforementioned poor CAM WORD is offered.
[0020] this invention to two or more CAM WORD Moreover, in addition, FR pulley decoder holding the address information of the poor CAM WORD which is the associative memory which carried the CAM WORD of the reserve as a redundant circuit, and is contained in two or more aforementioned CAM WORD, The CAM WORD of the aforementioned reserve is used according to the address information of the poor CAM WORD currently held at this FR pulley decoder. The shift control circuit controlled to shift the address of the aforementioned CAM WORD by the side of the high order (or low rank) address rather than the aforementioned poor CAM WORD, Control of the aforementioned shift control circuit is followed at the time of access of the read/write of data. The 1st shift circuit which shifts the i addresses of the aforementioned CAM WORD by the side of the high order (or low rank) address at a time to a high order (or low rank) address side rather than the aforementioned poor CAM WORD of eye i (i is one or more integers) watch, Control of the aforementioned shift control circuit is followed at the time of reference operation. The associative memory characterized by having the 2nd shift circuit which shifts the i addresses of the aforementioned CAM WORD by the side of the high order (or low rank) address at a time to a low rank (or high order) address side rather than the i-th aforementioned poor CAM WORD is offered.
[0021]
[Embodiments of the Invention] Below, based on the suitable example shown in an attached drawing, the associative memory of this invention is explained in detail.
[0022] Drawing 1 is the composition schematic diagram of one example of the associative memory of this invention. The associative memory (henceforth CAM) 10 shown in this drawing has the function to replace poor CAM WORD with the CAM WORD of the reserve as a redundant circuit, and to relieve it, and is equipped with the CAM array 12, the low decoder 14, FR pulley decoder 16, a fail low decoder and the shift control circuit 18, two shift circuits 20a and 20b, and priority encoders 22.
[0023] usual CAM WORD R0, R1, R2, --, R255 for 256 word (256Row) first specified in CAM10 of the example of illustration in the address which the CAM array (CAM Array) 12 followed -- in addition, it has CAM WORD (Redundancy) R256 of the redundant reserve for 1 word this example gives and explains the example which used the CAM array of the same composition so that comparison with CAM62 which applies the conventional redundant circuit shown in drawing 9 may become easy.
[0024] In addition, although this example explains noting that CAM WORD R0 is the CAM WORD of the most significant, it becomes low-ranking CAM WORD below at order in CAM WORD R1, R2, and R3 and the order of -- and CAM WORD R255 is the CAM WORD of the least significant this invention may not be limited to this, but may make CAM WORD R0 the least significant, may make it the CAM WORD of a high order below at order in CAM WORD R1, R2, and R3 and the order of --, and may constitute the CAM array 12 for CAM WORD R255 as CAM WORD of the most significant..
[0025] Below, in order of, the low decoder (Row Decorder) 14 decodes the logical address [7:0], i.e., address signal ADR inputted from the outside, and outputs the WORD selection signal for specifying the CAM WORD corresponding to this. From the low decoder 14, 256 WORD selection signals respectively corresponding to CAM WORD R0, R1, R2, --, R255 are outputted, and let only one WORD selection signal corresponding to address signal ADR [7:0] be an active state.
[0026] FR pulley decoder 16 holds the address of this poor CAM WORD, when the information whether poor CAM WORD exists, and poor CAM WORD exist. From this FR pulley decoder 16, the signal FAILADR [7:0] in which the address of poor CAM WORD is expressed as signal REDUN_EBL showing whether poor CAM WORD exists is outputted.
[0027] The composition of this FR pulley decoder 16 constitute FR pulley decoder 16 using a fuse, and for example, by cutting a fuse according to the address of the corresponding poor CAM WORD May

specify the memory address and Or the internal register is prepared, if it is a means by which the address of poor CAM WORD -- the address of poor CAM WORD may be stored in this internal register -- can be specified, it is not limited at all but each well-known means can use conventionally.
[0028] According to signal REDUN_EBL and Signal FAILADR [7:0], a fail low decoder and the shift control circuit (Fail Row Decoder & Shift Control) 18 use spare CAM WORD, and they output the shift control signal which controls operation of the shift circuits 20a and 20b so that the address of the CAM WORD by the side of the high order address may be shifted rather than poor CAM WORD. In this example, a shift control signal is inputted into both shift circuits 20a and 20b, and the fail low decoder and the shift control circuit 18 are shared in the shift circuits 20a and 20b.
[0029] Shift circuit (Shift Circuit) 20a by the side of a decoder [whether according to control of a shift control signal, 256 WORD selection signals inputted through a fail low decoder and the shift control circuit 18 from the low decoder 14 are outputted as they are, and] Or every one WORD selection signal corresponding to all the CAM WORD by the side of the low rank address is shifted to the CAM WORD by the side of the low rank address rather than poor CAM WORD. That is, the address of all the CAM WORD by the side of the low rank address is shifted to a low rank address side rather than poor CAM WORD.
[0030] On the other hand, shift circuit 20b by the side of an encoder [whether similarly, 256 reference coincidence output signals by the side of the high order address of the 257 reference coincidence output signals inputted through a coincidence line by control of a shift control signal from each CAM WORD of the CAM array 12 are outputted as they are, and] Or every one reference coincidence output signal corresponding to all the CAM WORD by the side of the low rank address is shifted to the CAM WORD by the side of the high order address rather than poor CAM WORD. That is, the address of all the CAM WORD by the side of the low rank address is shifted to a high order address side rather than poor CAM WORD.
[0031] Here, when poor CAM WORD does not exist (signal REDUN_EBL=0), it is controlled so that the logical address and the physical address which are CAM WORD are in agreement. That is, 256 WORD selection signals outputted from the low decoder 14 are inputted into CAM WORD R0, R1, R2, --, R255 which corresponds respectively as they are, and the reference coincidence output signal outputted from CAM WORD R0, R1, R2, --, R255 is also inputted into a priority encoder 22 as it is.
[0032] On the other hand, when poor CAM WORD exists (signal REDUN_EBL=1), according to Signal FAILADR [7:0], every one WORD selection signal corresponding to all the CAM WORD by the side of the low rank address is shifted to the CAM WORD by the side of the low rank address rather than poor CAM WORD. Moreover, every one reference coincidence output signal corresponding to all the CAM WORD by the side of the low rank address is shifted to the CAM WORD by the side of the high order address rather than poor CAM WORD.
[0033] Finally, about 256 reference coincidence output signals inputted from shift circuit 20b, according to predetermined priority, a priority encoder (Priority Encoder) 22 encodes the memory address which is the CAM WORD by which coincidence was detected one by one, and outputs this one by one as the ranking hit address HHA of the highest priority [7:0]. Though it is not limited at all, for example, the priority of CAM WORD has so high that it is the CAM WORD by the side of the low rank address or the high order address priority, it is good.
[0034] In addition, neither the number of WORD of a CAM array nor the number of bits of the CAM cell contained in 1 word is limited at all. Moreover, although it could be prepared what word and is arranged to the memory address by the side of the least significant in the example of illustration, even if it arranges to the memory address by the side of the most significant or arranges spare CAM WORD to other memory addresses, it is easy to be natural [WORD]. Moreover, each thing of well-known composition can use the low decoder 14 and a priority encoder 22 conventionally.
[0035] When the CAM WORD of two or more reserves is prepared, here in shift circuit 20a by the side of a decoder Every one address of the CAM WORD by the side of the low rank address is shifted to a low rank address side rather than the 1st poor CAM WORD. Every two addresses of the CAM WORD by the side of the low rank address are shifted to a low rank address side rather than the 2nd poor CAM

WORD. It is necessary to shift the i addresses of the CAM WORD by the side of the low rank address at a time to a low rank address side like the following rather than the poor CAM WORD of eye i (i is one or more integers) watch.
[0036] When the CAM WORD of two or more reserves is prepared, moreover, in shift circuit 20b by the side of an encoder Every one address of the CAM WORD by the side of the low rank address is shifted to a high order address side rather than the 1st poor CAM WORD. It is necessary to shift every two addresses of the CAM WORD by the side of the low rank address to a high order address side rather than the 2nd poor CAM WORD, and to shift the i addresses of the CAM WORD by the side of the low rank address at a time to a high order address side rather than the i-th poor CAM WORD like the following.
[0037] Next, two shift circuits 20a and 20b are explained more to the fail low decoder shown in drawing 1 and the shift control circuit 18, and a row at a detail.
[0038] Drawing 2 is the composition schematic diagram of one example of the shift circuit by the side of a decoder at the fail low decoder and shift control circuit row which are used by the associative memory of this invention. As shown in this drawing, the fail low decoder and the shift control circuit 18 are equipped with the control circuit 24 prepared respectively corresponding to the poor CAM WORD selection signal. Moreover, shift circuit 20a by the side of a decoder is equipped with the selector 26 prepared corresponding to each CAM WORD R0, R1, R2, --, R256.
[0039] Here, the reversal signal SFTNi of the poor CAM WORD selection signal FRi which corresponds respectively, and the shift control signal outputted from the control circuit (control circuit corresponding to the poor CAM WORD selection signal by the side of the 1-word high order address) 24 of the preceding paragraph is inputted into each control circuit 24 of a fail low decoder and the shift control circuit 18. Moreover, the shift control signal SFTi outputted from each control circuit 24 is inputted into the selection terminal of a selector 26 with which shift circuit 20a corresponds respectively.

[0040] In addition, the poor CAM WORD selection signal FRi is a signal which decodes the signal FAILADR showing the address of poor CAM WORD [7:0], and is acquired. When all the poor CAM WORD selection signals FRi are inactive when, as for the poor CAM WORD selection signal FRi, poor CAM WORD does not exist in the case of this example, on the other hand poor CAM WORD exists, only one poor CAM WORD selection signal FRi will be in an active state.
[0041] Moreover, WORD selection-signal Wi-1 corresponding to the CAM WORD by the side of 1 high order address is inputted into each selector 26 of shift circuit 20a as the WORD selection signal Wi corresponding to each CAM WORD R0, R1, R2, --, R256. Moreover, the shift control signal SFTi is inputted into the selection terminal of each selector 26 from the control circuit 24 which corresponds respectively as above-mentioned, and the output signal GWi of each selector 26 is inputted into the CAM WORD which corresponds respectively.
[0042] In a fail low decoder and the shift control circuit 18, when poor CAM WORD does not exist, the shift control signal SFTi outputted from each control circuit 24 is inactive. According to this, the WORD selection signal Wi corresponding to each CAM WORD Ri is outputted from each selector 26 as a WORD signal GWi by shift circuit 20a.
[0043] On the other hand, when poor CAM WORD exists, the shift control signal SFTi outputted from the control circuit 24 corresponding to all the poor CAM WORD selection signals FRi by the side of the low rank address containing the poor CAM WORD selection signal FRi of an active state will be in an active state. According to this, WORD selection-signal Wi-1 corresponding to the CAM WORD by the side of 1 high order address is outputted as a WORD signal GWi from each selector 26.
[0044] That is, as shown intelligibly for the conceptual diagram of drawing 3 , there is the usual CAM WORD to P0-P6, and it presupposes that there is P7 which is spare CAM WORD. Here, supposing poor CAM WORD is P3, the WORD selection signals L0-L2 which correspond respectively will be inputted into CAM WORD P0-P2. Poor CAM WORD P3 is fixed to a low level, and the WORD selection signals L3-L6 respectively shifted one [at a time] are inputted into CAM WORD P4-P7.
[0045] Here, the example shown in drawing 4 is given and the shift circuit by the side of a decoder is

further explained to a fail low decoder and a shift control circuit row at a detail.
[0046] As shown in drawing 4 (a), each control circuit 24 of a fail low decoder and the shift control circuit 18 consists of the OR gate 28 and an inverter 30. The reversal signal SFTNi of the poor CAM WORD selection signal which corresponds respectively, and the shift control signal outputted from the control circuit 24 of the preceding paragraph is inputted into two inversed input terminals of the OR gate 28. Moreover, from the OR gate 28, the shift control signal SFTi is outputted and the reversal signal SFTNi is outputted through the inverter 30.
[0047] Moreover, each selector 26 of shift circuit 20a by the side of a decoder consists of the two AND gates 32 and 34, the NOR gates 36, inverters 38, and buffers 40. The WORD selection signal Wi corresponding to each CAM WORD Ri and the shift control signal SFTi outputted from the OR gate 28 of a control circuit 24 which corresponds respectively are inputted into two inversed input terminals of the AND gate 34. On the other hand, WORD selection-signal Wi-1 corresponding to CAM WORD Ri-1 by the side of 1 high order address and reversal signal SFTNi-1 of the shift control signal outputted from the inverter 30 of the control circuit 24 of the preceding paragraph are inputted into two inversed input terminals of the AND gate 32. Moreover, both the output signals of the AND gates 32 and 34 are inputted into the NOR gate 36, and the output signal of the NOR gate 36 is outputted as a WORD signal GWi through the inverter 38 and the buffer 40.
[0048] When poor CAM WORD does not exist in the circuit shown in drawing 4 (a), in the poor CAM WORD selection signal and the example of illustration which decode Signal FAILADR [7:0] and are acquired, all the output signals of NAND gate 42 become high-level. Moreover, when poor CAM WORD does not exist, the reversal signal SFTN0 of the shift control signal of the most-significant address is high-level, and, in the output signal SFTi of the OR gate 28, i.e., all shift control signals, a low level and the output signal SFTNi of an inverter 30, i.e., the reversal signal of a shift control signal, become high-level altogether.
[0049] Therefore, since the output signal of the AND gate 32 into which the reversal signal SFTNi of a shift control signal is inputted serves as a low level, the WORD selection signal Wi outputted from the low decoder 14 is outputted from the AND gate 34 into which the shift control signal SFTi is inputted, and it is outputted as a WORD signal GWi through the NOR gate 36, an inverter 38, and a buffer 40.
[0050] On the other hand, when poor CAM WORD exists, only the poor CAM WORD selection signal which decodes Signal FAILADR [7:0] and is obtained serves as a low level. Thereby, the shift control signal SFTi corresponding to all the CAM WORD by the side of the low rank address containing this poor CAM WORD selection signal FRi becomes high-level, and the reversal signal SFTNi serves as a low level altogether.
[0051] therefore, in the selector 26 corresponding to all the CAM WORD by the side of the low rank address containing the poor CAM WORD selection signal of a low level Since the output signal of the AND gate 34 into which the shift control signal SFTi is inputted serves as a low level Are outputted from the AND gate 32 into which the reversal signal SFTNi is inputted to the low decoder 14. WORD selection-signal Wi-1 corresponding to the CAM WORD by the side of 1 high order address is outputted, and it is outputted as a WORD signal GWi through the NOR gate 36, an inverter 38, and a buffer 40.
[0052] In addition, in the selector 26 corresponding to all the CAM WORD by the side of the high order address, the shift control signal SFTi serves as a low level, and the reversal signal SFTNi is still altogether more high-level than the poor CAM WORD selection signal of a low level. Therefore, by the selector 26 corresponding to all the CAM WORD by the side of the high order address, it operates completely like the case where poor CAM WORD does not exist, rather than the poor CAM WORD selection signal of a low level.
[0053] Drawing 4 (b) is the component-circuit view of an example of the conventional low decoder. This drawing shows a part for 1 word of the low decoder used by the conventional CAM which has not applied redundant circuit technology, in order to make intelligible the scale of the additional circuit concerning this invention. Here, NAND gate 44, an inverter 38, and a buffer 40 are equivalent to NAND gate 44, an inverter 38, and a buffer 40 in the circuit concerning this invention shown in drawing 4 (a),

respectively.
[0054] The additional portions of the circuit concerning this invention are only the OR gate 28 and the inverter 30 equivalent to a control circuit 24, and the two AND gates 32 and 34 and the NOR gate 36 equivalent to a selector 26 so that clearly, if the circuit shown in this drawing 4 (a) and (b) is compared. These circuits are circuits added to the conventional CAM shown in drawing 8 , if compared with the additional circuit in the conventional CAM shown in drawing 9 , the circuit scale is extraordinarily small and the output time delay is also very short.
[0055] Then, drawing 5 is the composition schematic diagram of one example of the shift circuit by the side of an encoder at the fail low decoder and shift control circuit row which are used by the associative memory of this invention. As shown in this drawing, the composition of a fail low decoder and the shift control circuit 18 is the same as that of what is shown in drawing 2 . Moreover, shift circuit 20b by the side of an encoder is equipped with the selector 46 prepared corresponding to each CAM WORD R0, R1, R2, --, R255.
[0056] In addition, in the example shown in drawing 5 , in order to make an understanding easy, the fail low decoder and the shift control circuit 18 are formed also in the preceding paragraph of shift circuit 20b by the side of an encoder. Thus, the shift control signal SFTi and its reversal signal SFTNi are taken about, a fail low decoder and the shift control circuit 18 connect, and you may make it share a fail low decoder and the shift control circuit 18 in both, as you may prepare in the shift circuits 20a and 20b by the side of a decoder and an encoder individually, respectively and it is shown in drawing 1 .
[0057] In shift circuit 20b shown in drawing 5 , reference result output signal OROUTi+1 corresponding to the CAM WORD by the side of the reference result output signal OROUTi corresponding to each CAM WORD R0, R1, R2, --, R256 and 1 low rank address is inputted into each selector 46. Moreover, the shift control signal SFTi which corresponds respectively is inputted into the selection terminal of each selector 46, and the output signal PRIi of each selector 46 is inputted into the priority encoder 22.
[0058] Operation of a fail low decoder and the shift control circuit 18 is as above-mentioned. That is, when poor CAM WORD does not exist, the shift control signal SFTi outputted from each control circuit 24 is inactive. According to this, the reference result output signal OROUTi corresponding.to each CAM WORD Ri is outputted from each selector 46 as a signal PRIi by shift circuit 20b.
[0059] On the other hand, when poor CAM WORD exists, the shift control signal SFTi outputted from the control circuit 24 corresponding to all the poor CAM WORD selection signals FRi by the side of the low rank address containing the poor CAM WORD selection signal FRi of an active state will be in an active state. According to this, reference result output signal OROUTi+1 corresponding to the CAM WORD by the side of 1 low rank address is outputted as a signal PRIi from each selector 46.
[0060] That is, as shown intelligibly for the conceptual diagram of drawing 6 , there is the same usual CAM WORD to P0-P6, there is P7 which is spare CAM WORD, and supposing poor CAM WORD is P3, the reference result output signal of CAM WORD P0-P2 will be outputted as signals L0-L2 as it is. Moreover, the reference result output signal of CAM WORD P3 is disregarded, and every one reference result output signal of CAM WORD P4-P7 is shifted respectively, and is outputted as signals L3-L6.
[0061] Here, the example shown in drawing 7 is given and the shift circuit by the side of a decoder is further explained to a fail low decoder and a shift control circuit row at a detail.
[0062] As shown in drawing 7 (a), each control circuit 24 of a fail low decoder and the shift control circuit 18 is completely the same as what is shown in drawing 4 (a). Therefore, as already stated, the portion surrounded with the dashed line of drawing 7 (a) can be used with shift circuit 20a by the side of a decoder in common, and as shown in drawing 1 , from a fail low decoder and the shift control circuit 18, the shift control signal SFTi and its reversal signal SFTNi may be taken about, and it may connect.
[0063] Moreover, each selector 46 of shift circuit 20b by the side of an encoder is constituted by two tri-state inverters 48 and 50. The reference result output OROUTi of the CAM WORD which corresponds respectively is inputted into the tri-state inverter 48, reference result output OROUTi+1 of the CAM WORD by the side of 1 low rank address is inputted, wye yard connection is made and both output signal is outputted to the tri-state inverter 50 as a signal PRIi.
[0064] Moreover, the shift control signal SFTi (output signal of the OR gate 28) which corresponds

respectively is inputted into the control inversed input terminal of the tri-state inverter 48, and the control-input terminal of the tri-state inverter 50, and the reversal signal SFTNi of the shift control signal which corresponds respectively is inputted into the control-input terminal of the tri-state inverter 48, and the control inversed input terminal of the tri-state inverter 50. That is, according to the state of the shift control signal SFTi and its reversal signal SFTNi, only either turns off ON and another side.
[0065] In the circuit shown in drawing 7 (a), when poor CAM WORD does not exist, as already stated, in all poor CAM WORD selection signals and examples of illustration, all the output signals of NAND gate 42 become high-level. Moreover, the reversal signal SFTN0 of the shift control signal of the most-significant address is high-level, and, in the output signal SFTi of the OR gate 28, i.e., all shift control signals, a low level and the output signal SFTNi of an inverter 30, i.e., the reversal signal of a shift control signal, become high-level altogether.
[0066] Therefore, the tri-state inverter 48 as which the reversal signal SFTNi of a shift control signal is inputted into the control-input terminal turns on, and since the tri-state inverter 50 as which the shift control signal SFTi is inputted into the control-input terminal turns off, the reference result output OROUTi of the CAM WORD which corresponds respectively is outputted as a signal PRIi.
[0067] On the other hand, when poor CAM WORD exists, as similarly stated already, only the poor CAM WORD selection signal (output signal of a NAND gate) which decodes Signal FAILADR [7:0] and is obtained serves as a low level. Thereby, the shift control signal SFTi corresponding to all the CAM WORD by the side of the low rank address containing this poor CAM WORD selection signal FRi becomes high-level, and the reversal signal SFTNi serves as a low level altogether.
[0068] Therefore, in the selector 46 corresponding to all the CAM WORD by the side of the low rank address containing the poor CAM WORD selection signal of a low level, the tri-state inverter 50 as which the shift control signal SFTi is inputted into the control-input terminal turns on, and since the tri-state inverter 48 as which the reversal signal SFTNi of a shift control signal is inputted into the control-input terminal turns off, reference result output OROUTi+1 of the CAM WORD by the side of 1 low rank address is outputted as a signal PRIi.
[0069] In addition, in the selector 46 corresponding to all the CAM WORD by the side of the high order address, the shift control signal SFTi serves as a low level, and the reversal signal SFTNi is still altogether more high-level than the poor CAM WORD selection signal of a low level. Therefore, by the selector 46 corresponding to all the CAM WORD by the side of the high order address, it operates completely like the case where poor CAM WORD does not exist, rather than the poor CAM WORD selection signal of a low level.
[0070] Drawing 7 (b) is the component-circuit view of an example of the output section by the side of the conventional encoder. This drawing shows a part for the output section by the side of the encoder used by the conventional CAM which has not applied redundant circuit technology, i.e., 1 word of the reference result output of each CAM WORD, in order to make intelligible the scale of the additional circuit concerning this invention. Here, an inverter 52 is equivalent to the tri-state inverter 48 in the circuit concerning this invention shown in drawing 7 (a).
[0071] Supposing the additional portion of the circuit concerning this invention shares the circuit portion equivalent to a control circuit 24, it is only the tri-state inverter 50 which constitutes a selector 46, so that clearly, if the circuit shown in this drawing 7 (a) and (b) is compared. This circuit is a circuit added to the conventional CAM shown in drawing 8 , if compared with the additional circuit in the conventional CAM shown in drawing 9 , the circuit scale is extraordinarily small and the output time delay is also very short.
[0072] As mentioned above, in CAM of this invention, the scale of the circuit which changes mutually the logical address (address inputted from the outside) and a physical address (address actually used inside) is small. and since neither size comparison nor addition and subtraction is necessarily performed each time at the time of access of the read/write of stored data, and reference operation unlike CAM using the redundant circuit technology of the conventional method, even if it compares with the conventional CAM in which the redundant circuit is not established, an output time delay is an EQC mostly

[0073] The associative memory of this invention is fundamentally above. As mentioned above, although the associative memory of this invention was explained in detail, of course in the range which this invention is not limited to the above-mentioned example, and does not deviate from the main point of this invention, you may make various improvement and change.
[0074]
[Effect of the Invention] As explained to the detail above, it replaces the reference coincidence output of spare CAM WORD, and the reference coincidence output of poor CAM WORD while the associative memory of this invention holds the address information of the poor CAM WORD contained in two or more CAM WORD, controls it according to the address information of this poor CAM WORD to replace poor CAM WORD and spare CAM WORD and replaces the address of poor CAM WORD, and the address of spare CAM WORD. Thereby, without increasing a circuit scale and an output time delay according to the associative memory of this invention, it can be used being able to replace poor CAM WORD and spare CAM WORD, and the yield of a product can be raised.

CLAIMS

[Claim(s)]

[Claim 1] The associative memory which carried the CAM WORD of the reserve as a redundant circuit in addition to two or more CAM WORD characterized by providing the following FR pulley decoder holding the address information of the poor CAM WORD contained in two or more aforementioned CAM WORD The 1st shift control circuit controlled to use the CAM WORD of the aforementioned reserve and to shift the address of the aforementioned CAM WORD by the side of the high order (or low rank) address rather than the aforementioned poor CAM WORD according to the address information of the poor CAM WORD currently held at this FR pulley decoder The 1st shift circuit which shifts the i addresses of the aforementioned CAM WORD by the side of the high order (or low rank) address at a time to a high order (or low rank) address side according to control of the shift control circuit of the above 1st rather than the aforementioned poor CAM WORD of eye i (i is one or more integers) watch at the time of access of the read/write of data The CAM WORD of the aforementioned reserve is used according to the address information of the poor CAM WORD currently held at the aforementioned FR pulley decoder. The 2nd shift control circuit controlled to shift the address of the aforementioned CAM WORD by the side of the high order (or low rank) address rather than the aforementioned poor CAM WORD, The 2nd shift circuit which shifts the i addresses of the aforementioned CAM WORD by the side of the high order (or low rank) address at a time to a low rank (or high order) address side rather than the i-th aforementioned poor CAM WORD according to control of the shift control circuit of the above 2nd at the time of reference operation

[Claim 2] The associative memory which carried the CAM WORD of the reserve as a redundant circuit in addition to two or more CAM WORD characterized by providing the following FR pulley decoder holding the address information of the poor CAM WORD contained in two or more aforementioned CAM WORD The shift control circuit controlled to use the CAM WORD of the aforementioned reserve and to shift the address of the aforementioned CAM WORD by the side of the high order (or low rank) address rather than the aforementioned poor CAM WORD according to the address information of the poor CAM WORD currently held at this FR pulley decoder The 1st shift circuit which shifts the i addresses of the aforementioned CAM WORD by the side of the high order (or low rank) address at a time to a high order (or low rank) address side according to control of the aforementioned shift control circuit rather than the aforementioned poor CAM WORD of eye i (i is one or more integers) watch at the time of access of the read/write of data The 2nd shift circuit which shifts the i addresses of the aforementioned CAM WORD by the side of the high order (or low rank) address at a time to a low rank (or high order) address side rather than the i-th aforementioned poor CAM WORD according to control of the aforementioned shift control circuit at the time of reference operation

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[Translation done.]